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CONTENTS

Vertical Deflection Amplifier for 150MHz Oscilloscope 158–166

Horizontal Deflection Amplifier for 150MHz Oscilloscope 167–174

Schmitt Trigger as Level Detector: Analysis and Performance of FCL101 175–181

Light Units in SI 182–184

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VOLUME 10 NUMBER 95 September 1968

Contents

Vertical Deflection Amplifier for 150MHz Oscilloscope
S. Sijtstra 158

Horizontal Deflection Amplifier for 150MHz Oscilloscope
K. Hart and F. G. Oude Moleman 167

Schmitt Trigger as Level Detector:
Analysis and Performance of FCL101
P. A. Neeteson 175

Light Units in SI
F. A. Sowan 182

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Vertical Deflection Amplifier for 150MHz Oscilloscope

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The circuit of a deflection amplifier for an oscilloscope is described, the bandwidth being 150MHz. Except for cathode followers incorporated in the probe and the vertical shift control from which the inputs are derived, this direct-coupled amplifier makes use of transistors throughout. The circuit is substantially symmetrical and shunt feedback is alternated with series feedback in successive stages to make high (GB)-products available and obviate the need for emitter followers. Use of a cascode output stage ensures an adequate voltage swing and minimises the capacitance presented to the delay networks which are needed for driving successive pairs of deflection electrodes in the cathode-ray tube. Buffer amplifiers to supply the trigger take-off for the horizontal sweep are incorporated.

INTRODUCTION

The evolution of the cathode-ray oscilloscope from a merely qualitative to an accurately quantitative instrument has greatly increased the range of its uses and, concomitantly, the demands placed on it by its users. Not only is there a continuing demand for still higher sensitivity and accuracy but also for greater bandwidth. Where only regularly recurring wave-forms are to be dealt with, the actual limitations on bandwidth can sometimes be circumvented, as in sampling oscilloscopes, although at the cost of substantially increasing the complexity of the instrument. Fortunately, however, recent improvements in transistors now make it possible to design amplifier circuits for wide-band oscilloscopes without recourse to sampling techniques.

This article describes a vertical deflection amplifier having a bandwidth of 150MHz and a deflection sensitivity of 5mV/cm with the D13-450GH/01 cathode-ray tube. (A compatible horizontal deflection amplifier is described in Ref. 1.)

GENERAL DESCRIPTION OF CIRCUIT

The amplifier is direct-coupled throughout. Use of a push-pull design affords symmetrical drive of deflection electrodes and at the same time simplifies the biasing of the several stages. The block diagram is given in Fig. 1.

Signals picked off by the probe are fed to the phase-splitter preamplifier which incorporates both the gain adjustment and the vertical shift control. The delay-line driver matches the symmetrical output of the preamplifier to the characteristic impedance (93Ω) of the two delay lines; it also incorporates the calibration control and the buffer stage for the trigger take-off. After having been delayed 150ns (to ensure satisfactory display of leading edges) the signals are applied via the output driver to the output stage which drives the vertical deflection electrodes of the cathode-ray tube. Except as noted in the following summary descriptions of the several circuits, BFY90 transistors are used throughout.

To avoid loading the signal source, the input impedance of the probe must be high over the entire range of operating frequencies; in addition, there must be no risk that the

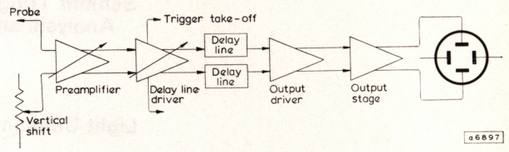

Fig. 1—Block diagram of complete amplifier

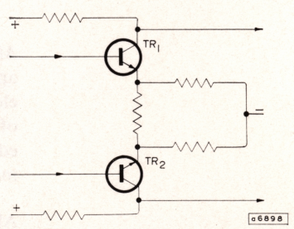

Fig. 2—Basic circuit of first stage of pre-amplifier (long-tailed pair)

signal source or the probe itself will be damaged if the latter accidentally comes into contact with high voltages. To satisfy these requirements an active probe of a type described in Ref. 2 is used.Using an EC1000 subminiature triode connected as a cathode follower, the probe is linked to the amplifier by a 75Ω coaxial cable. The voltage gain is 0·5 and the bandwidth 440MHz (rise time 0·8ns).

In the phase-splitter preamplifier, the first stage is a long-tailed pair with series feedback in the emitter circuit (Fig. 2); in the second stage shunt feedback from the collector to the base is used. This combination of alternating series and shunt feedback, as illustrated by Fig. 3, is particularly well-suited for wide-band applications and is used throughout the amplifier; amongst other advantages, it obviates the need for emitter followers and makes high (GB)-products obtainable. The phase-splitter preamplifier provides a voltage gain of 9 and a bandwidth of 440MHz (rise time 0·8ns).

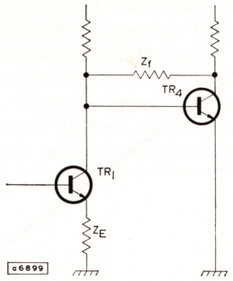

Fig. 3—Basic circuit of two-stage amplifier with combined series and shunt feedback

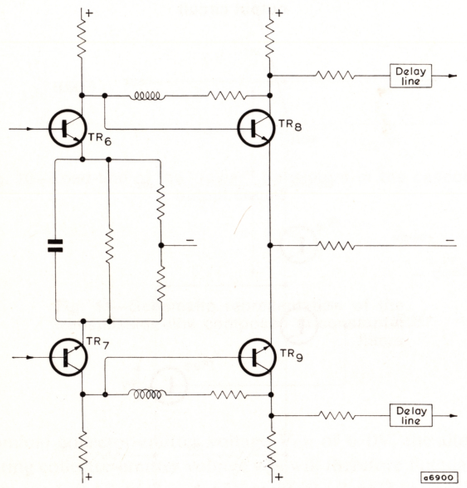

Fig. 4—Basic circuit of delay-line driver

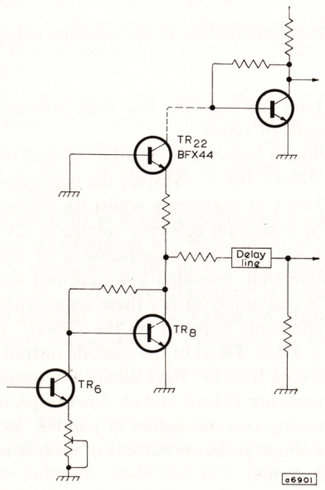

Fig. 5—Connection of buffer stage (BFX44) to the delay-line driver for trigger take-off

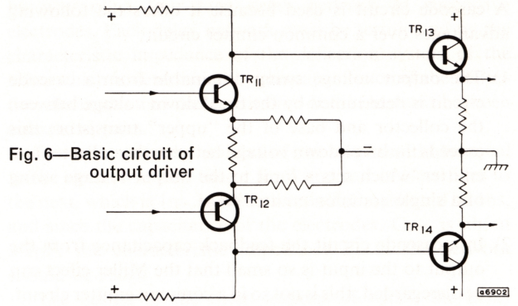

Fig. 6—Basic circuit of output driver

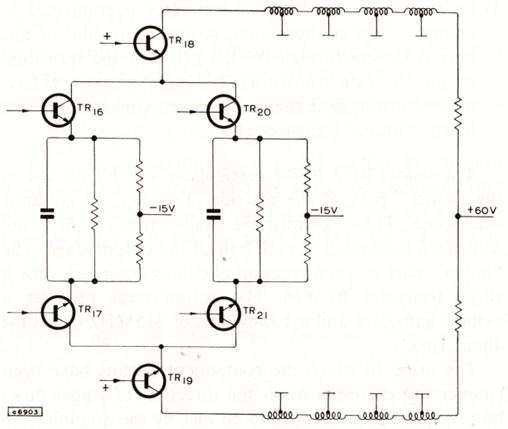

Fig. 7—Basic circuit of output stage

A similar series-shunt feedback pair is used for the delay line driver (Fig. 4). A gain calibration potentiometer in the common emitter circuit of the first stage makes it possible to adjust the sensitivity up to a maximum of 5mV/cm. The voltage gain is 9 and the bandwidth is once more 440MHz (rise time 0·8ns).

To keep the trigger take-off from loading the delay line driver, buffer amplifiers with high input impedance are used (Fig. 5). The first transistor of each of these combines with the output transistor of the delay line driver to form a cascode circuit incorporating series feedback; shunt feedback is again used in the second stage (transistor BFX44, not discussed here).

In the output driver (Fig. 6) which terminates the delay lines, the first two transistors are connected in common emitter configuration and the second two are arranged as emitter followers to provide a low impedance source for the output stage. The voltage gain is 3 and the bandwidth almost 600MHz (rise time 0·6ns). The maximum peak-to-peak value of the output signal is 2×2·5V.

Though the overall bandwidth required is 150MHz, it is important for all stages preceding the output stage to have a very much larger bandwidth. This is because the bandwidth of the output stage itself is necessarily limited (as will be shown later) to about 300MHz.

The basic circuit of the output stage is shown in Fig. 7.

A cascode circuit is used because it offers the following advantages over a common emitter circuit:

1) The output voltage swing obtainable from a cascode circuit is determined by the breakdown voltage between the collector and base of the "upper" transistor; this exceeds the breakdown voltage between the collector and emitter, which sets a limit to the output voltage swing of a single common emitter stage.

2) In a cascode circuit the feedback capacitance from the output to the input is so small that the Miller effect can be disregarded; this is not so in a common emitter circuit.

3) In a cascode the "upper" transistor is connected in common base configuration, so the bandwidth of this part is extremely high (of the order of the transition frequency of the transistor). The high-frequency behaviour of the stage is therefore governed almost entirely by the "lower" transistor.

Transistors BFW30 are particularly suitable for use in the "lower" part of the cascode. To keep the collector dissipation within permissible limits, two of them are connected in parallel in each half of the output stage. The "upper" part of each cascode circuit is equipped with a single transistor BFW16. The output stage provides a voltage gain of 8 and a bandwidth of 315MHz (rise time about 1ns).

The order in which the component circuits have been enumerated corresponds to the direction of signal flow; however, the requirements to be met by the amplifier are imposed not so much by the signals to be dealt with as by the cathode-ray tube on which they are to be displayed. In the following particular discussion of the circuits and design considerations, the reverse order will therefore be followed, starting with the output circuit and working back towards the probe.

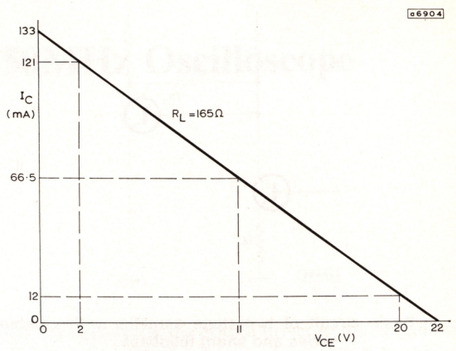

Fig. 8—Load-line of the "upper" transistors in the cascode output circuit

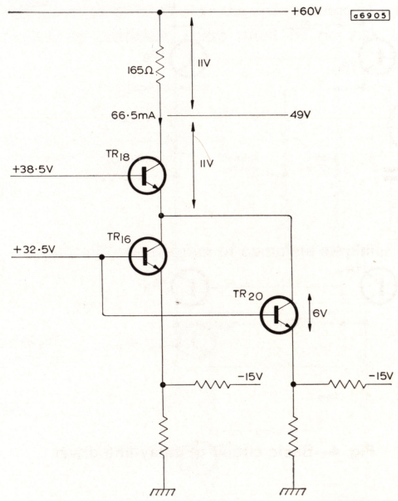

Fig. 9—Voltage distribution across cascode output circuit

CIRCUIT DESIGN DETAILS

The various parts of the circuit are discussed in detail below, beginning at the output end.

D.C. Performance of Output Stage

For full scan the "upper" transistors (TR_{18}, TR_{19}) of both halves of the cascode output stage should provide an output voltage swing of 30V, to which 20% should be added for overscan, so the total required is V_o = 36V; that is, 18V from each half of the push-pull output stage.

The current swing necessary for obtaining this voltage clearly depends on the characteristic impedance of the D13-450GH/01 cathode-ray tube. This amounts to 330Ω between the vertical deflection electrodes, and so the required current swing I_o is 36/330 = 109mA. Allowance must be made to prevent non-linearity at either end of the current range: this could be caused by the decrease of the transition frequency at low collector currents and voltages.

Fig. 8 shows the load line ($R_L = \frac{1}{2}Z_o = 165\Omega$) in the I_c-V_{CE} plane. To guard against bottoming or cutting off the transistor, collector voltage margins of 2V have been allowed at both the high and low ends, corresponding to current margins of 12mA.

The maximum collector dissipation of each transistor is $V_s^2/4R_L = 22^2/4 \times 165 = 734$mW; the maximum collector current is 133mA at bottoming whilst its average value is 66·5mA. The maximum collector voltage is 22V when the transistor is cut off. The specifications of the BFW16 transistor show that, provided it is equipped with a small cooling fin, it can amply satisfy these requirements.

The requirements imposed on the "lower" transistors (TR_{16}, TR_{17}, TR_{20}, TR_{21}) of the cascode output stage can be determined as follows. Here again, the maximum and average currents are 133mA and 66·5mA respectively (Fig. 8). By connecting two transistors in parallel, as shown in Fig. 9, the average collector current of each is reduced to 66·5/2 = 33·25mA.

To obtain a voltage gain of 8, the emitter resistor of each transistor should be $2R_L/8 = 2 \times 165/8 \simeq 40\Omega$; for

low frequencies the input impedance of the "upper" transistor (TR_{18}) may be disregarded. The load line for $R_L = 40\Omega$ has been drawn in Fig. 10.

The current may range from 12/2 = 6mA to 121/2 = 60·5mA (Fig. 8). When the "upper" transistor is bottomed, the current of 133/2 = 66·5mA will produce a voltage drop of 0·0665 × 40 = 2·66V across the load resistance. At a

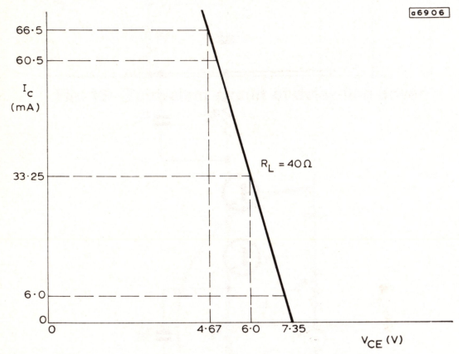

Fig. 10—Load-line of the "lower" transistors in the cascode output circuit

nominal collector-emitter voltage V_{CE} of 6·0V, the alternating collector-emitter voltage v_{CE} will therefore fluctuate between 6·0−2·66/2 = 4·67V and 6·0+2·66/2 = 7·33V.

The maximum dissipation amounts to $V_s^2/4R_L = 7.33^2/4 \times 40 \simeq 340$mW, which will occur at $v_{CE} = (0.340 \times 40)^{\frac{1}{2}} = 3.7$V. Now Fig. 10 suggests that since the minimum value of v_{CE} is 4·67V, the maximum dissipation is given by the product of this voltage and the corresponding current, that is 4·67 × 66·5 = 310mW.

At high frequencies the input resistance $r_{bb'}$ of the upper transistor may assume a value up to 15Ω, raising the total load resistance; but this will occur only momentarily and so there is no need to design the circuit for more than 310mW.

The transistor BFW30 can therefore be made to satisfy the imposed requirements by the addition of a heatsink. The thermal resistance of the BFW30 for junction to case is 0·5degC/mW, and if the transistor is mounted on a heatsink of thermal resistance 30degC/W then the maximum ambient temperature is calculated as follows:

$$T_{amb(max)} = 200 - [(0.5 + 0.03) \times 310] = 35°C. \quad \ldots(1)$$

Interelectrode Delay Network

The y-deflection electrodes of the D13-450GH/01 cathode-ray tube are sectioned into four axially spaced pairs. To drive the pairs in correct phase relation with each other the output from each half of the amplifier is applied by way of a four-stage delay network to successive electrodes. Each delay network must be terminated by the characteristic impedance of the deflection system of the tube, which is determined by the capacitance of the deflection electrodes and the transit time of the electrons between successive pairs.

For each network the delay of one stage should be equal to the electron transit time τ from one pair of electrodes to the next, which is 1ns. In other words Z_oC_{def} should be 1ns, and since the capacitance of the electrodes, C_{def}, is about 3·2pF, the characteristic impedance Z_o of the network should be 330Ω.

The design of the filter sections of which the delay networks are composed is based on the following considerations (Fig. 11):

1) The wiring from the deflection electrodes to the series coils L_s has a self-inductance of about 15nH.

2) The interconnection of the coils $L_c/2$ introduces a self-inductance of about 10nH.

For a constant-k filter $L_k = C_kZ_o^2$ (Ref. 3), which in this instance amounts to 95·5nH. It can be calculated that with a single-layer air-core coil the coupling factor k of the two coil halves can reach a value of up to 0·62. The value

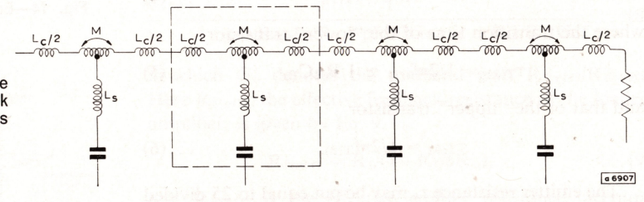

Fig. 11—Schematic representation of the transmission-line composed of constant-k filters

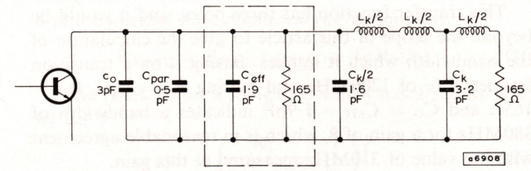

Fig. 12—Termination of c.r.t. filter sections

of M (plus the effect of L_c and L_s) in the equivalent circuit is just about 1, so that a constant-k section is obtained. Each coil consists of three turns of 1mm (or s.w.g. 20) enamelled copper wire closely wound on a former with a diameter of 7·5mm.

A.C. Performance of Output Stage

The high transition frequency of transistor BFW16 makes its high-frequency behaviour satisfactory for the purpose. From the capacitance of the deflection electrodes (3·2pF) and the characteristic impedance of the delay network (165Ω, see Fig. 12) it follows that the cut-off frequency is 700MHz. Since this is far in excess of the bandwidth of the output stage (about 300MHz), the impedance at the input of the delay network may safely be regarded as a resistance of 165Ω. Because a filter section is terminated at its input side when it is current driven by

half a constant-k section, a capacitance of $C_k/2 = 3{\cdot}2/2 = 1{\cdot}6$pF (at M = 1) forms part of the input of the filter. Subtracted from the total capacitance at the collector of the transistor, which is approximately 4pF since the value of C_{par} is negligible this gives a residual effective capacitance C_{eff} of $4{\cdot}0-1{\cdot}6 = 2{\cdot}4$ pF; this, together with the characteristic impedance of 165Ω, determines the bandwidth at the output of the cascode circuit (Fig. 13). For this RC-combination the gain is 3dB down at a frequency of $1/2\pi RC \simeq 400$MHz, which means that the output circuit does not seriously affect the total bandwidth of this stage.

Now the transfer function of the cascode circuit will be investigated with reference to Fig. 14. This function can be expressed by the equation,

$$\frac{v_o}{v_i}(p) = \frac{R_C}{R_E+r_e+(r_{bb'}+R_s)/\beta} \times \frac{1}{(1+Kp\tau_{T(1)})(1+p\tau_{T(2)})(1+Ap\tau_{T(1)})}. \quad \ldots(2)$$

In Eq.2

$$K = \frac{r_{bb'}+R_s}{R_E+r_e+(r_{bb'}+R_s)/\beta}, \quad \ldots(3)$$

and

$$A = R_C C_C/\tau_{T(1)}, \quad \ldots(4)$$

where the transition time of the "lower" transistor

$$\tau_{T(1)} = 1/2\pi f_{t(1)} \simeq 1/R_E C_E, \quad \ldots(5)$$

and that of the "upper" transistor

$$\tau_{T(2)} = 1/2\pi f_{T(2)}. \quad \ldots(6)$$

The emitter resistance r_e may be put equal to 25 divided by the direct current expressed in milliamps.

This transfer function has three poles, and it would be beyond the scope of this article to give the calculation of the bandwidth which it implies. Basing it on a transition frequency f_T of 1200MHz and putting $R_E = 40\Omega$, $R_C = 165\Omega$ and $C_C = C_{eff} = 1{\cdot}9$pF indicates a bandwidth of 380MHz for a gain of 8, which is in reasonable agreement with the value of 310MHz measured at this gain.

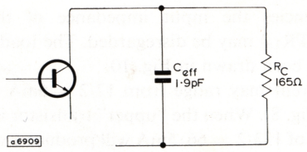

Fig. 13—Loading of the output stage

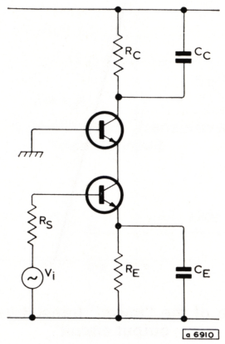

Fig. 14—Equivalent circuit used for calculation of transfer function of cascode circuit

Output Driver

At an output stage gain of 8, the push-pull input required for obtaining an output of 40V is $2\times 2{\cdot}5$V, which is rather a large signal for the driver to supply.

As shown in Fig. 15, each half of the output driver consists of two stages: transistor TR_{11}, which operates in push-pull with its counterpart in the opposite half, and the emitter follower TR_{13}.

Transistor TR_{11}, which is connected in common emitter configuration, is biased for a direct current of 12·5mA. Its load resistance is formed by a 150Ω resistor in series with a bypassed 820Ω resistor. This arrangement makes it easy to match the required d.c. level of the output stage. Moreover, since the collector voltage is about half the supply voltage, the arrangement minimises the effect of d.c. level variations (shift) on the power dissipated by the transistor and on its temperature drift.

Transistor TR_{13} is biased for a direct current of 10mA.

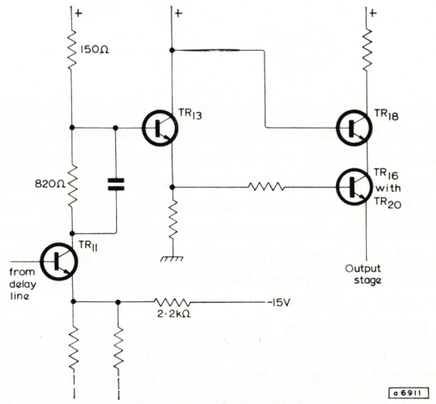

Fig. 15—Output driver

The "lower" transistors of the cascode output stage are connected to its emitter; its collector is connected to the same supply source as the base of the "upper" transistor of the output stage.

The overall gain of the output driver amounts to 3, so the peak-to-peak input signal it requires for full drive of the output stage is 1·67V.

Interstage Delay Line

The delay line preceding the driver stage consists of 30m of coaxial cable with a characteristic impedance of 93Ω.

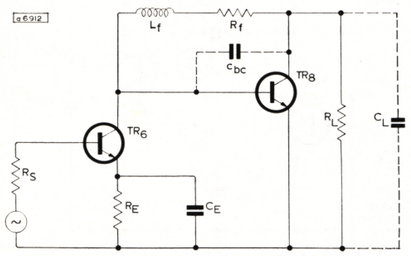

Fig. 16—Equivalent circuit of delay-line driver

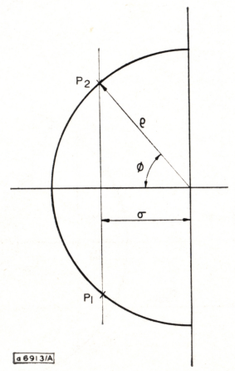

Fig. 17—Pole configuration of delay-line driver

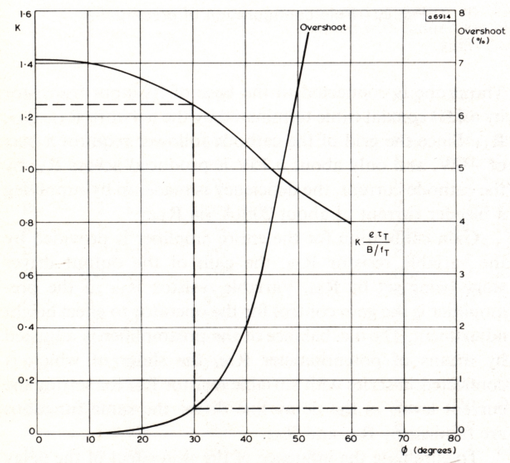

Fig. 18—Overshoot, and $K = \rho\tau/(B/f_t)$ plotted as functions of phase angle ϕ

It introduces a delay of 150ns. The performance of this type of delay line is such that it can be used for frequencies up to 400MHz without complex correction networks having to be used.

Delay Line Driver

The delay line driver (Fig. 16), which also provides the trigger take-off, makes use of one transistor, TR_6, with series feedback, followed by another, TR_8, with shunt feedback (Ref.4). This arrangement is particularly suitable for driving an ohmic load such as that presented by the delay line. Analysis of its performance is based on three assumptions:

1) The load capacitance C_L is so small that X_L may be put equal to R_L over the frequency range under consideration.

2) The reactance of the collector-to-base capacitance c_{bc} is high compared to the impedance of the feedback network formed by L_f, R_f.

3) The emitter resistance R_E is much larger than $(r_{bb'} + R_S)/\beta$.

The circuit must be so dimensioned that the following two conditions are satisfied. Firstly, the time constant $R_E C_E \simeq \tau_T$ should be equal to $1/2\pi f_t$. Secondly, the time constant of the feedback network should be equal to:

$$\tau_f = L_f/R_f = \{(r_{bb'} + R_s)/R_{E(eff)}\}\tau_T. \quad \ldots(7)$$

Under these conditions only one pair of complex poles remains in the transfer function (Fig. 17), which is then given by

$$\frac{v_o}{v_1} = \frac{1}{1+p\tau_T R_{f(eff)}/R_L + p^2\tau_T^2 G_o(r_{bb'}+R_s)/R_L.G_o}, \quad \ldots(8)$$

in which G_o denotes the midband gain $R_{f(eff)}/R_{E(eff)}$. Here $R_{f(eff)}$, the effective feedback resistance of the loaded amplifier, is given by Eq. 9,

$$R_{f(eff)} = R_f/(1+R_f/\beta R_L), \quad \ldots(9)$$

and $R_{E(eff)}$ is the effective emitter resistance, account being taken of the influence of the source resistance R_s and the internal base resistance $r_{bb'}$ as follows:

$$R_{E(eff)} = R_E + r_e + (r_{bb'} + R_s)/\beta. \quad \ldots(10)$$

The poles lie on a semicircle which has a radius given by Eq. 11.

$$\rho\tau_T = \left(\frac{R_L}{r_{bb'}+R_S}.\frac{1}{G_o}\right)^{\frac{1}{2}}. \quad \ldots(11)$$

With the aid of the graph shown in Fig. 18, in which the overshoot, and K, which equals $\rho\tau_T/(B/f_T)$, have been plotted as functions of ϕ, it is possible to determine the overshoot and the bandwidth with respect to the transition frequency f_T of the transistor by making use of Eq. 12 and Eq. 13.

$$(f_t/B) = K\left(\frac{r_{bb'}+R_s}{R_L}.G_o\right)^{\frac{1}{2}}, \quad \ldots(12)$$

$$R_f = 2(\cos\phi/K)(B/f_t)R_L. \quad \ldots(13)$$

The graph shows that at $\phi = 30°$ the overshoot will be 0·5% and $K = 1{\cdot}22$. Substituting in the above formulae $R_L = 82\Omega$, $R_s = 47\Omega$, $r_{bb'} = 25\Omega$, $\beta \simeq h_{FE} = 40$, $r_e = 25/I_C = 2{\cdot}5\Omega$, and $G_o = 9$, whence $(f_t/B) = 3{\cdot}4$, $R_f = 470\Omega$ and $R_E = 49\Omega$. This means that for a bandwidth of 400 MHz the transition frequency should exceed 1·380GHz, whilst C_E should be 2·3pF and L_f should have a value of 100nH.

Phase Splitter and Preamplifier

The operation of the phase splitter and preamplifier is now discussed with reference to Fig. 19. This circuit, which has also been described in Ref. 3, differs from that used for the delay line driver in the configuration of the feedback circuit of transistor TR_4. The feedback impedance Z_f is here formed by a resistor R_f connected in parallel with a capacitor C_f, as is customary with a mainly capacitive load. The transfer function of the circuit is given by the following equation.

$$\frac{v_o}{v_i} = G_o \cdot \frac{1}{1 + p\tau_T(r_{bb'} + R_s)/R_{E(eff)}} \times$$

$$\times \frac{1}{1+p\{R_fC_f+\tau_T(R_f+R_L)/R_L+T_{eq}/\beta\}+p^2T_{eq}\tau_T}, \quad \ldots(14)$$

where

$$T_{eq} = R_f(C_f + C_L), \quad \ldots(15)$$

it being assumed that τ_T equals R_EC_E.

This transfer function has three poles, of which two are complex and one is situated on the real axis. The two poles of the shunt part lie on a circle whose radius is given by the equation,

$$\rho\tau_T = \left(\frac{\tau_t}{\tau_f}\cdot\frac{1}{1+C_L/C_f}\right)^{\frac{1}{2}}, \quad \ldots(16)$$

the projection of which on the real axis is given by,

$$\sigma_{sh}\tau_T = -\frac{1 + (1 + R_f/R_L)\tau_T/\tau_f + (1 + C_L/C_f)/\beta}{2(1 + C_L/C_f)} \ldots(17)$$

The pole of the series-feedback stage lies on the real axis, its position being given by the equation

$$\sigma_{ser}\tau_T = R_{E(eff)}/(r_{bb'} + R_s). \quad \ldots(18)$$

If this pole is situated at a distance corresponding to three times the overall frequency from the origin (see Fig. 20), its influence may be disregarded. The behaviour of the stage is then determined solely by the pair of complex poles. For a gain of $G_o = 9$ the required component values can then be calculated to be $R_f = 470\Omega$ and $R_E = 49\Omega$, the bandwidth being 400MHz.

The high-frequency performance is determined by the feedback capacitance C_f and the capacitance C_E across the emitter circuit. The capacitance C_f should be 2·3pF, and so the 1·5pF collector capacitance c_e of transistor BFY90 needs to be augmented by a capacitance of 0·8pF. However, since the potentiometer for adjusting the gain is included in the emitter circuit, the 0·8pF is supplied by the stray capacitance and no additional capacitor is called for.

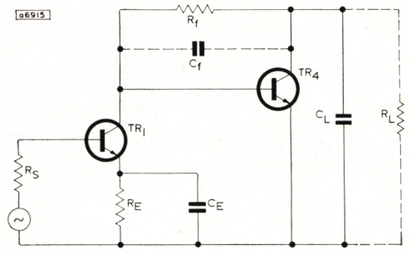

Fig. 19—Equivalent circuit used for investigating the transfer function of the phase-splitter and preamplifier

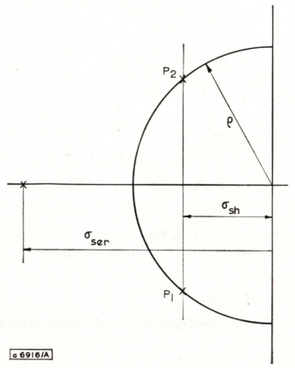

Fig. 20—Pole configuration of preamplifier

COMPLETE CIRCUIT DIAGRAM

Figs. 21 and 22 show the circuit of the entire amplifier.

Input signals to both sides of the preamplifier are derived. from two EC1000 triodes operating as cathode followers, one providing vertical shift control and the other being incorporated in the probe. The lead from the vertical shift control to the base of the corresponding input transistor is passed through a Ferroxcube bead to avoid instability. The probe is connected to the base of its input transistor by a 75Ω coaxial cable terminated by the network R_{11}, R_{12}, R_{14}. Since the grid of the cathode follower requires a bias of −2V, and only about 0·75V is produced across R_{12} by the cathode current, the deficiency is made up by supplying a bleeder current of about 20mA via R_{14}.

Gain calibration for the entire amplifier is provided by the variable resistor R_{33}, the gain of the output driver stage being set by R_{55}. Variable resistor R_{18} in the preamplifier is the gain control for the operator to effect height adjustment. The d.c. balance of the preamplifier is adjusted by means of potentiometer R_{23}, the slider of which is connected in series with variable resistor R_{21} for setting the current level; in the delay line driver the same functions are fulfilled by R_{41} and R_{43}.

To eliminate the influence of the skin effect of the delay line on the pulse response, the common emitter resistor of transistors TR_6 and TR_7 is bypassed by two RC networks.

Transistor TR_3 serves merely as a low-resistance supply source for feeding transistors TR_1, TR_4, TR_6 and their partners TR_2, TR_5 and TR_7. Similarly, transistor TR_{10} feeds transistors TR_{11} and TR_{12} of the output driver, whilst transistor TR_{15} feeds the emitter followers (TR_{13} and TR_{14}) and supplies the base current of the "upper" transistors (TR_{18} and TR_{19}) of the output cascode. To avoid interaction and instability, the base leads are also passed through Ferroxcube beads.

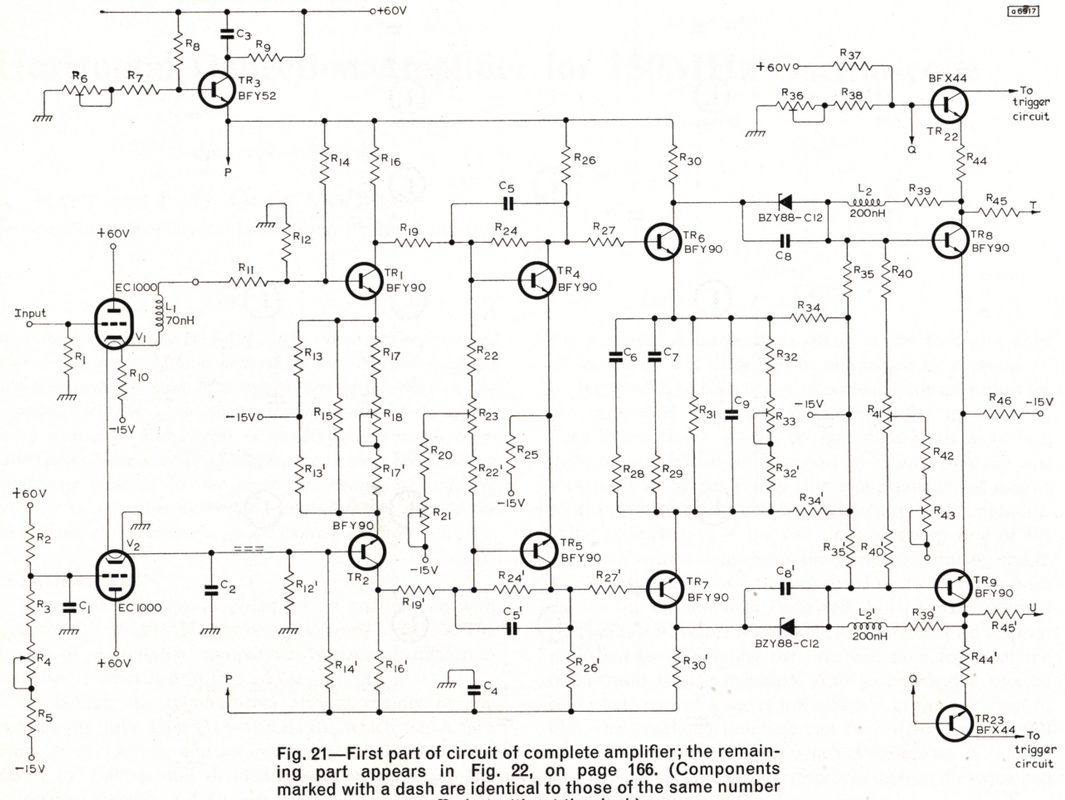

Fig. 21—First part of circuit of complete amplifier; the remaining part appears in Fig. 22, on page 166. (Components marked with a dash are identical to those of the same number suffix but without the dash)

R_1	1	MΩ,	⅛W	R_{30}	330	Ω,	¼W	R_{59}	68	Ω,	⅛W
R_2	820	Ω,	¼W	R_{31}	180	Ω,	¼W	R_{60}	68	Ω,	⅛W
R_3	56	kΩ,	⅛W	R_{32}	56	Ω,	⅛W	R_{61}	1·2	kΩ,	3W
R_4	10	kΩ,	pot. w.w.	R_{33}	500	Ω,	pot. w.w.	R_{62}	82	Ω,	¼W
R_5	150	kΩ,	¼W	R_{34}	2·7	kΩ,	¼W	R_{63}	2	kΩ,	pot. w.w.
R_6	2	kΩ,	pot. w.w.	R_{35}	1·8	kΩ,	¼W	R_{64}	5·6	kΩ,	¼W
R_7	1	kΩ,	¼W	R_{36}	500	Ω,	pot. w.w.	R_{65}	4·7	kΩ,	¼W
R_8	2·2	kΩ,	¼W	R_{37}	2·2	kΩ,	1W	R_{66}	820	Ω,	5W
R_9	200	Ω,	5W	R_{38}	1	kΩ,	1W	R_{67}	82	Ω,	⅛W
R_{10}	13	Ω,	½W	R_{39}	470	Ω,	¼W	R_{68}	1·2	kΩ,	3W
R_{11}	10	Ω,	⅛W	R_{40}	820	Ω,	¼W	R_{69}	165	Ω,	2W
R_{12}	75	Ω,	⅛W	R_{41}	500	Ω,	pot. w.w.	C_1	0·1	μF	
R_{13}	1·5	kΩ,	¼W	R_{42}	270	Ω,	¼W	C_2	10	nF	
R_{14}	3·3	kΩ,	½W	R_{43}	500	Ω,	pot. w.w.	C_3	10	nF	
R_{15}	270	Ω,	⅛W	R_{44}	330	Ω,	¼W	C_4	10	nF	
R_{16}	1·8	kΩ,	⅛W	R_{45}	47	Ω,	⅛W	C_5	0·8	pF	
R_{17}	56	Ω,	⅛W	R_{46}	1	kΩ,	¼W	C_6	22	pF	
R_{18}	1	kΩ,	pot. w.w.	R_{47}	2	kΩ,	pot. w.w.	C_7	15	pF	
R_{19}	47	Ω,	½W	R_{48}	4·7	kΩ,	¼W	C_8	10	nF	
R_{20}	270	Ω,	¼W	R_{49}	5·6	kΩ,	¼W	C_9	25	pF	
R_{21}	200	Ω,	pot. w.w.	R_{50}	1	kΩ,	5W	C_{10}	25	pF	
R_{22}	820	Ω,	¼W	R_{51}	56	Ω,	⅛W	C_{11}	10	nF	
R_{23}	500	Ω,	pot. w.w.	R_{52}	93	Ω,	⅛W	C_{12}	10	nF	
R_{24}	470	Ω,	½W	R_{53}	150	Ω,	¼W	C_{13}	10	nF	
R_{25}	1	kΩ,	¼W	R_{54}	820	Ω,	¼W	C_{14}	0·1	μF	
R_{26}	560	Ω,	¼W	R_{55}	500	Ω,	pot. w.w.	C_{15}	10	nF	
R_{27}	47	Ω,	⅛W	R_{56}	180	Ω,	⅛W	C_{16}	10	nF	
R_{28}	82	Ω,	⅛W	R_{57}	2·2	kΩ,	1W	C_{17}	1	pF	
R_{29}	68	Ω,	⅛W	R_{58}	2·7	kΩ,	¼W	C_{18}	1	pF	

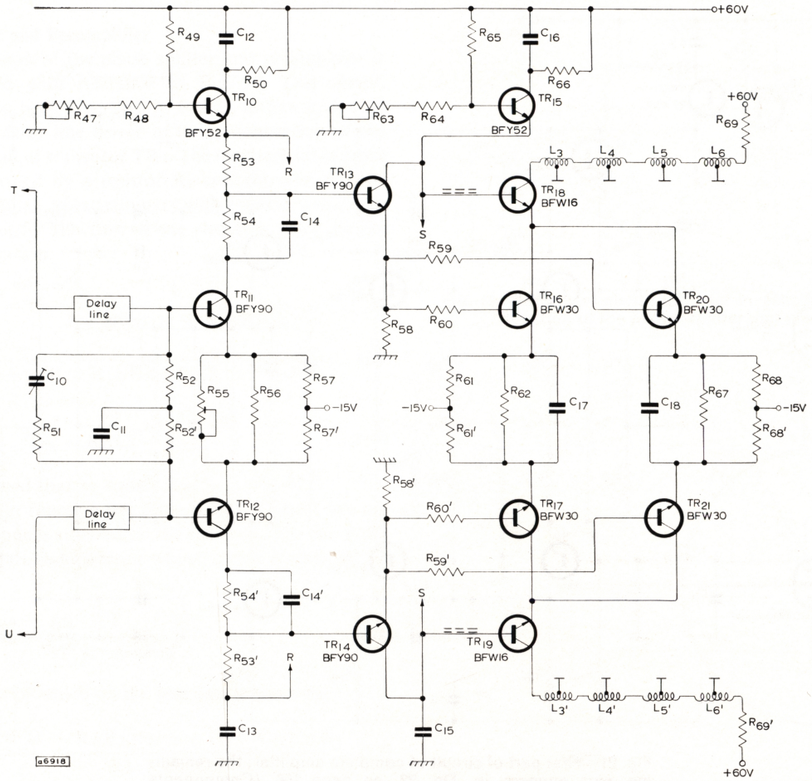

Fig. 22—Second part of circuit of complete amplifier; the first part appears in Fig. 21 on page 165.

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Horizontal Deflection Amplifier for 150MHz Oscilloscope

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With cathode-ray tube D13-450GH/01 the amplifier described provides a linear 130mm deflection; for detailed study of fast transients the scale of a chosen part of the trace can be expanded tenfold, a maximum tracing speed of 0·5ns/mm being available. The circuit is largely symmetrical, long-tailed pairs being used in all stages, but to meet the differing conditions imposed by the need for signals of opposite polarity to drive the deflection electrodes, one side of the output stage is augmented by an emitter follower.

INTRODUCTION

A vertical deflection amplifier for an oscilloscope with a bandwidth of 150MHz has been described in Ref. 1. The design of a suitable compatible horizontal deflection amplifier is described in this article.

As before, the requirements are set mainly by the cathode-ray tube type D13–450GH/01, which has a face diameter of 130mm, and an internal graticule measuring 60mm by 100mm and divided at 10mm intervals. The deflection sensitivity is 1·8V/mm, and so a sweep of $13 \times 18 = 234$V would be required to traverse the full diameter; to avoid distortion within the 100mm of the graticule, this would have to be linear over a range of $10 \times 18 = 180$V. If a sweep of more than 234V is made available to begin with, however, it is easier to ensure the required linearity; the principal non-linearities occur at the foot and crest of the ramp, and these can be eliminated by clipping.

Bandwidth as such is not so critical a consideration for the horizontal deflection amplifier as for the vertical. Techniques which would be inadmissible in a vertical deflection amplifier can be used to ensure that the one waveform to be dealt with (the rising portion of a sawtooth) meets the requirements of linearity and amplitude. What is important is the rise time or sweep rate of the sawtooth, which determines the horizontal tracing speed. For general purposes a tracing speed of 5ns/mm has been chosen for the amplifier described, but to make selected parts of fast waveforms available for more detailed display, provision for expanding the timebase by a factor of ten (0·5ns/mm) is also included. And to enable the user to select that part of a waveform which is of most interest to him, the expanded timebase can be shifted over the full span of the sawtooth from which it is derived. A voltage step with a rise time of 3·5ns displayed against the expanded timebase is shown in Fig. 1.

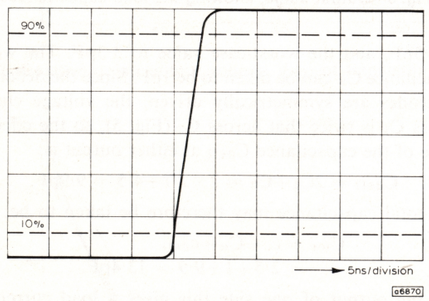


Fig. 1—Display of a voltage step with a rise time of 3·5ns against the expanded timebase

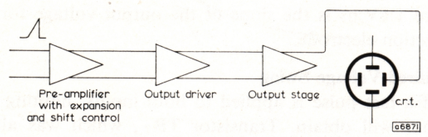


Fig. 2—Block diagram of the amplifier

GENERAL DESCRIPTION OF DESIGN

A functional block diagram of the horizontal deflection amplifier is given in Fig. 2. It consists of a two-stage pre-amplifier, a driver, and an output stage.

Fig. 3 shows the basic circuit of the preamplifier. It consists of a phase-inverting amplifier preceded by two emitter followers, one supplying the input sawtooth voltage and the other the control for shifting the relative

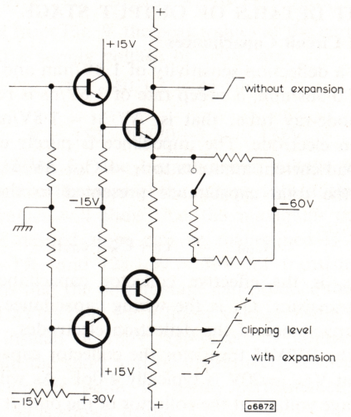


Fig. 3—Basic circuit of the phase inverter and preamplifier

position of the display when the expanded timebase is used. The provision for expanding the timebase is incorporated in the phase-inverting amplifier in the form of a low resistance shunt which can be switched across the common emitter resistor of the two transistors.

The basic circuit of the driver and output stages is shown in Fig. 4. The two driver transistors are connected as emitter followers, thus presenting a low impedance to the output stage. As in the preamplifier, transistors BSX20 are used in the driver stage. The output stage uses three BFW45 transistors. Voltage-dependent feedback, to be discussed later, is applied from the output to the driver transistors. Although the drive to the deflection electrodes is symmetrical, the amplifier that supplies it is not. A principal reason for this is the differing conditions imposed on the output transistors by the fact that one of them must supply a positive-going and the other a negative-going sweep voltage. Under quiescent conditions, that is before the start of an input signal, transistor TR_8 is almost cut off, whereas transistor TR_7 is almost bottomed. With the peak load required, this would impose unacceptable demands on the latter transistor. For this reason the emitter follower stage (transistor TR_9) has been provided which buffers transistor TR_7 against the x_1-deflection electrode capacitance and reduces its capacitive load appreciably. The current of the emitter follower itself is quite low when quiescent and is increased only by the positive-going sweep voltage. Transistor TR_8 requires no emitter follower, maximum output being obtained (as will be shown on page 170) by using a small emitter capacitor.

The basic circuit as shown would have a limitation in that the 1·8V/ns slope, being determined not by the bandwidth but by the available current and the capacitive load, cannot be maintained up to the full output voltage. Current must of course be limited, on account of both the dissipation limits of the transistors and the need to preserve linearity.

Since the required output at the deflection electrodes is the principal factor affecting the design, in the following more detailed discussion the individual circuits are discussed in the reverse order, working backwards from the output stage to the preamplifier.

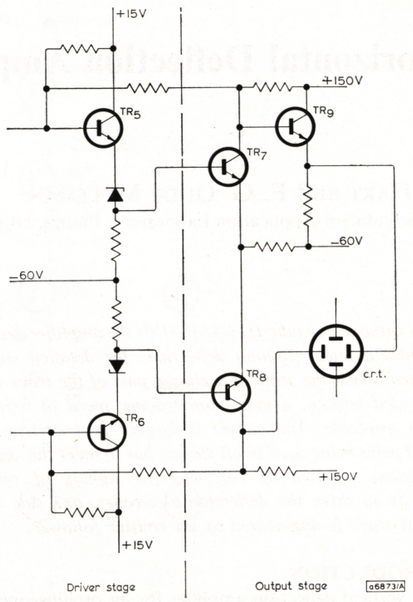


Fig. 4—Basic circuit of the driver and output stages

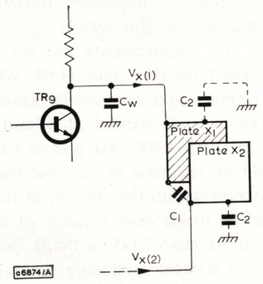


Fig. 5—Output stage, showing the load capacitances

CIRCUIT DETAILS OF OUTPUT STAGE

Effect of Circuit Capacitances

With a deflection sensitivity of 1·8V/mm and a tracing speed of 0·5ns/mm, a sweep rate of 3·6V/ns is required at the cathode-ray tube; that is, $\Delta V/\Delta t = 1{\cdot}8$V/ns at each deflection electrode. The impedance is purely capacitive, so the load current amounts to $i_L = C_{tot}.\Delta V/\Delta t$, in which C_{tot} is the total capacitance presented to the output; that is,

$$C_{tot} = c_c+C_w+c_{defl}, \qquad \ldots(1)$$

where c_c is the effective collector capacitance of the output transistor, C_w is the wiring capacitance and c_{defl} is the capacitance of the deflection electrodes.

For the BFW45 transistor the collector capacitance c_c quoted at $V_{CB} = 20$V is typically 4·0pF. As will be seen, the average voltage at the collector of the output transistor is 70V, which means that the typical value of c_c is reduced to 2·5pF, and the worst-case value to 3·3pF. The wiring capacitance C_w can be taken to be 1pF. Since the deflection electrodes are symmetrically driven, the voltage change across C_1 is twice that across C_2 (Fig. 5), so the effective value of the capacitance C_{defl} at either output is:

$$C_{defl} = 2C_1+C_2 = 2\times2{\cdot}7+4{\cdot}5 = 9{\cdot}9\text{pF}. \quad \ldots(2)$$

The total capacitance may therefore be taken to be:

$$C_{tot} = c_c+C_w+c_{defl} = 2{\cdot}5+1+9{\cdot}9 = 13{\cdot}4\text{pF}.$$

For the output of one side this gives a load current of

$$i_L = C_{tot}.\Delta V/\Delta t = 13{\cdot}4\times10^{-12}\times1{\cdot}8\times10^{9} \simeq 25\text{mA},$$

where 1·8V/ns is the slope of the output voltage for one deflection electrode.

Required Voltage Swing

If a fast pulse is applied to both inputs, limiting conditions will obtain. Transistor TR_7, which was almost bottomed, will move rapidly towards cut-off, its output

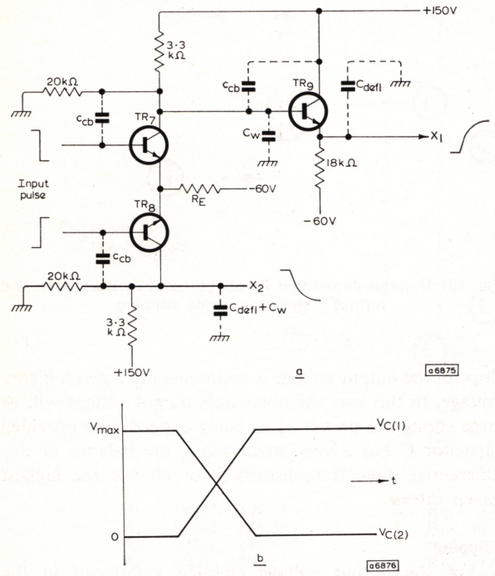


Fig. 6(a)—Detail of the output stage. The waveform of the output voltage $V_{C(1)}$ of transistor TR_7 and that of the output voltage $V_{C(2)}$ of transistor TR_8 are roughly indicated in (b)

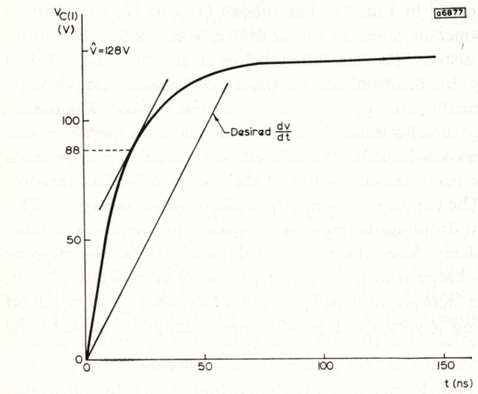


Fig. 7—Positive-going output voltage $V_{C(1)}$ of transistor TR_7

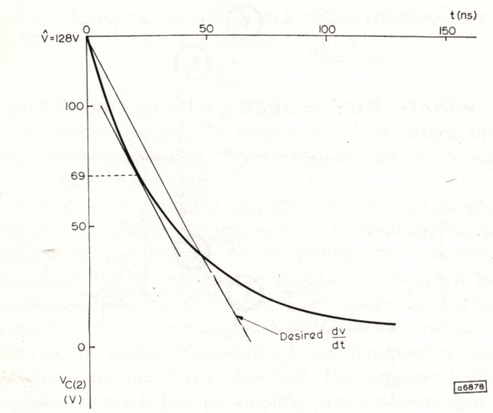


Fig. 8—Negative-going output voltage $V_{C(2)}$ of transistor TR_8

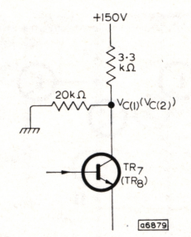


Fig. 9—Collector circuit of output transistors TR_7 and TR_8

going from almost zero to V_{max}; and transistor TR_8, which was almost cut off, will move towards bottoming, its output going from V_{max} almost to zero, the current through it being limited by the common emitter resistor R_E (see Fig. 6a). Denoting these voltages by $v_{C(1)}$ and $v_{C(2)}$ respectively, a situation as represented schematically in Fig. 6b will occur.

This is now investigated in greater detail with reference to Figs. 7 and 8. The output voltage $v_{C(1)}$ at the collector of transistor TR_7 and the current $i_{C(1)}$ through its load capacitance $C_{C(1)}$ are given by:

$$v_{C(1)} = \{1-\exp(-t/\tau_1)\}\hat{V}, \qquad \ldots(3)$$

and

$$i_{C(1)} = \{\exp(-t/\tau_1)\}\hat{I}, \qquad \ldots(4)$$

respectively, τ_1 being $R_{C(1)}C_{C(1)}$. Substituting for

$$R_{C(1)} = 3{\cdot}3\times20/(3{\cdot}3+20) = 2{\cdot}84\text{k}\Omega, \qquad \ldots(5)$$

and

$$C_{C(1)} = 2c_c+C_w = 2\times2{\cdot}5+1 = 6\text{pF}, \qquad \ldots(6)$$

gives:

$$\tau_1 = 2{\cdot}84\times10^{3}\times6\times10^{-12} = 17\text{ns}. \qquad \ldots(7)$$

Similarly, the output voltage $v_{C(2)}$ at the collector of transistor TR_8 and the resulting current $i_{C(2)}$ are:

$$v_{C(2)} = \{1-\exp(-t/\tau_2)\}\hat{V}, \qquad \ldots(8)$$

and

$$i_{C(2)} = \{\exp(-t/\tau_2)\}\hat{I}, \qquad \ldots(9)$$

respectively, where $\tau_2 = R_{C(2)}C_{C(2)}$. The resistance $R_{C(2)} = R_{C(1)} = 2{\cdot}84\text{k}\Omega$, but (as shown above) $C_{C(2)} = 13{\cdot}4$pF, and this gives:

$$\tau_2 = 2{\cdot}84\times10^{3}\times13{\cdot}4\times10^{-12} = 38\text{ns}. \qquad \ldots(10)$$

As follows from Fig. 9, the peak values of the current and voltage, at a supply voltage of 150V, are:

$$\hat{I} = 150/3{\cdot}3 = 45{\cdot}5\text{mA}, \qquad \ldots(11)$$

and

$$\hat{V} = 150\times20/(20+3{\cdot}3) = 128\text{V}. \qquad \ldots(12)$$

If the equation for the instantaneous voltage is differentiated to find the slope of the output, substitution of the relevant values will show that the maximum output at which the desired slope can be maintained is 88V for transistor TR_7 and 128—69 = 59V for transistor TR_8. This means that the output stage can produce the desired slope of 1·8V/ns only for a linear voltage swing of up to 88+59V instead of 180V. However, by applying feedback within the stage and by capacitively connecting the common emitter point to earth, performance can be improved, as is shown below.

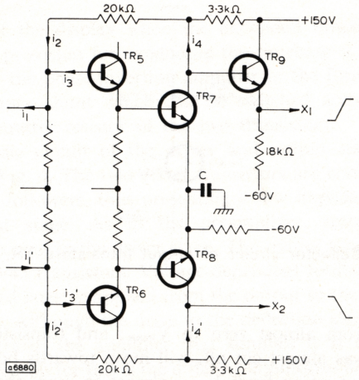


Fig. 10—Driver and output stages showing the method of feedback applied

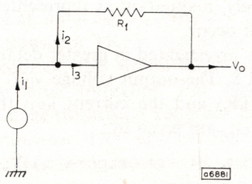


Fig. 11—Simplified circuit of the driver and output stages with negative feedback

Feedback

Fig. 10 shows the feedback used in the driver stages as well as the output stages. If voltage feedback were applied over a single stage it would substantially reduce the output current. However, by applying it over two stages the performance can be improved to the same extent, but now the feedback current i_2 is only a small proportion of i_4.

From Fig. 11 it will be seen that under steady conditions i_3 is negligible with respect to i_1, so that $i_1 \simeq i_2$ and the output voltage is $i_1 R_f$.

When a transient is applied at the input, the slope of the output voltage v_o is determined by the response of the amplifier; i_2 ceases to be equal to i_1 and therefore i_3 increases considerably. In the circuit of Fig. 10, this increased current will be further amplified by transistor TR_5 and provide almost unlimited current at the base of transistor TR_7. It is clear that the preceding stage must provide current drive if these conditions are to be fulfilled.

Use of an Emitter Capacitor

During a normal horizontal sweep pulse, transistor TR_7 provides a positive-going signal, the collector current being limited by the collector resistor. Transistor TR_8, on the other hand, providing a negative-going signal, has its collector current limited by the common emitter resistor.

If the emitter of TR_8 were earthed, its collector current (and thus the slope of the output voltage) could be greatly increased. By connecting a very small capacitor C between the common emitter point and earth (see Fig. 10), the same effect is achieved for high frequencies: the collector current of TR_8 is increased, and the desired

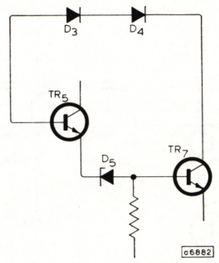


Fig. 12—Voltage-dependent feedback used in the driver and output stages to provide clipping

slope of the output voltage is maintained to a much higher voltage. In this way the obtainable output voltage will be large enough to permit of its being clipped, and provided capacitor C has a very small value, the balance of this differential stage is undisturbed for all but the highest sweep rates.

Clipping

For the output voltage clipping mentioned in the introduction, voltage-dependent feedback is used.

The basic circuit of the relevant section of the amplifier is shown in Fig. 12. The diodes D_3 and D_4 will start to conduct as soon as the collector-base voltage of output transistor TR_7 has fallen below a specific value. When they do, the feedback becomes very heavy, and virtually no further change occurs in the output voltage. The output stage then no longer operates as a difference amplifier with a very low impedance in the emitter circuit, this impedance now being raised to that of the common emitter resistor.

The clipping prevents the collector-base voltage of TR_7 from dropping below a given value, thus precluding turn-on delay. Since the stage is a differential one, the clipping also keeps transistor TR_8 from being completely cut off. (The incorporation of C_3 in Fig. 14 causes TR_7 to be cut off during a very short period approaching the peak of the

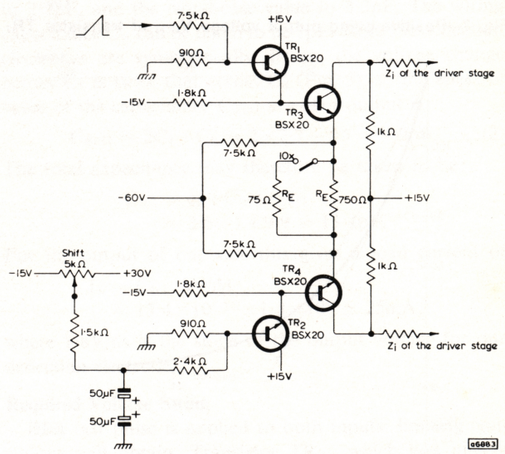
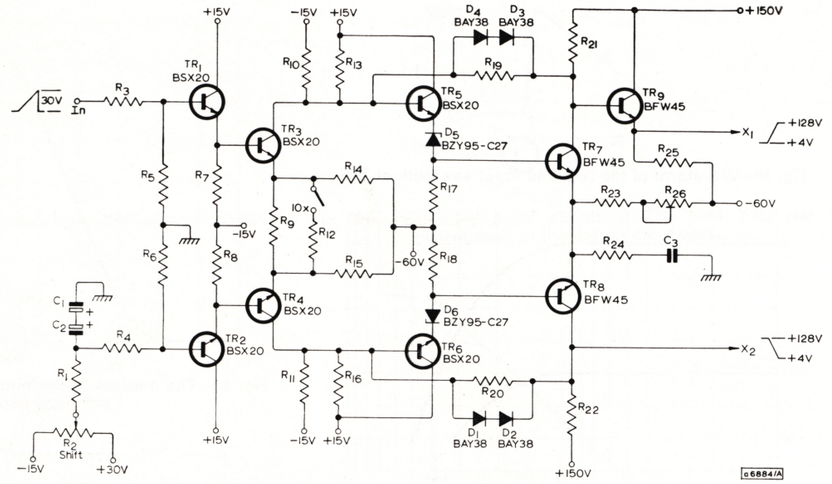


Fig. 13—Phase inverter and preamplifier

Fig. 14—Complete circuit of the amplifier



R_1	1·5kΩ,	¼W	R_{11}	3·9kΩ,	¼W	R_{21}	3·3kΩ,	5·5W
R_2	5 kΩ,	pot. w.w.	R_{12}	75 Ω,	¼W, ±1%	R_{22}	3·3kΩ,	5·5W
R_3	7·5kΩ,	¼W	R_{13}	1 kΩ,	¼W	R_{23}	680 Ω,	¼W
R_4	2·4kΩ,	¼W	R_{14}	7·5kΩ,	¼W	R_{24}	68 Ω,	¼W
R_5	910 Ω,	¼W	R_{15}	7·5kΩ,	¼W	R_{25}	18 kΩ,	5·5W
R_6	910 Ω,	¼W	R_{16}	1 kΩ,	¼W	R_{26}	250 Ω,	pot. w.w.
R_7	1·8kΩ,	¼W	R_{17}	2·2kΩ,	1W	C_1	50 μF,	25V
R_8	1·8kΩ,	¼W	R_{18}	15 kΩ,	¼W	C_2	50 μF,	25V
R_9	750 Ω,	¼W, ±1%	R_{19}	20 kΩ,	1W, ±1%	C_3	470 pF,	700V
R_{10}	3·9kΩ,	¼W	R_{20}	20 kΩ,	1W, ±1%			

sawtooth and allows TR_8 to supply the required current at the highest sweep rates.)

The voltage at which clipping occurs is determined by the zener voltage $V_{D(5)}$ (in this case 27V) of the voltage regulator diode D_5:

$$V_{CB(7)} = -V_{D(3)} - V_{D(4)} + V_{BE(5)} + V_{D(5)}$$
$$= -0{\cdot}6 - 0{\cdot}6 + 0{\cdot}7 + 27 = 26{\cdot}5V, \quad \ldots(13)$$

in which $V_{CB(7)}$ denotes the collector-base voltage of transistor TR_7 and $V_{BE(5)}$ the base-emitter voltage of TR_5. This voltage (26·5V) coincides with the specified h.f. knee voltage of the output transistor BFW45, which, according to the ratings, will not exceed 27V at a junction temperature of 120°C and a collector current of 50mA. The conditions here are a junction temperature of 140°C and a collector current of 44·5mA, which corresponds to an h.f. knee voltage not exceeding 26·5V.

CIRCUIT DETAILS OF PREAMPLIFIER STAGES

As well as providing the input to the driver stages, the preamplifier stages (Fig. 13) incorporate the provisions for x-expansion and shift.

It will be remembered that this section must supply current for driving the succeeding driver stage. Symmetrical emitter follower stages provide the necessary impedance transformation, the stages being balanced by a common 750Ω emitter resistor, which can be shunted by a smaller (75Ω) resistor to provide the tenfold x-expansion. The use of emitter followers ensures that neither the waveform nor the shift is distorted. The input sawtooth is applied to one half of the amplifier, and a potentiometer for the horizontal shift is connected to the other half.

Rise Time

The rise time of the preamplifier, which is limited mainly by the transistors of its second stage, is:

$$t_r = 2{\cdot}2[(R_S'/R_E+1)(1/\omega t + R_C c_c) + R_S' C_c], \quad \ldots(14)$$

where t_r is the rise time between 10% and 90% of the final value, and

$R_S' = R_S + r_{bb'} = R_i/h_{FE(1)} + r_{bb'}$
$= 910/40 + 50 = 73\Omega$,

R_E = emitter resistor (one side), being either 375Ω or 37Ω,

$\omega t = 2\pi f_T$, where f_T is the transistion frequency of transistors TR_3 and TR_4, that is 500MHz, which gives $\omega t = 3{\cdot}14 \times 10^9$,

R_C = collector load resistance formed by the 1kΩ collector resistor, paralled by the input impedance Z_i(210Ω) of the driver stage, giving 175Ω,

c_c = collector capacitance (3·3pF).

Without x-expansion ($R_E = 375\Omega$) the rise time is 2·9ns; with the expansion set at 10 ($R_E = 37\Omega$) the rise time is 7·5ns. Taking into account the rise time of the output stages, which is about 19ns, the rise time over the whole amplifier becomes:

$$t_r = (7{\cdot}5^2 + 19^2)^{\frac{1}{2}} \simeq 21\text{ns}, \quad \ldots(15)$$

which is in close agreement with the measured results given below.

Gain

The stage gain may be taken to be $R_C/(R_E + r_{oe})$; in this case r_{oe} is about 3Ω, so that without x-expansion a gain of 0·462, and, with expansion, a gain of 4·60 is obtained, providing the necessary expansion factor of 10.

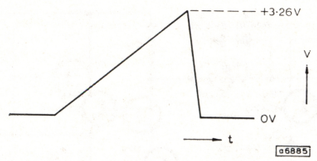


Fig. 15—Waveform of the required input sawtooth at TR_1

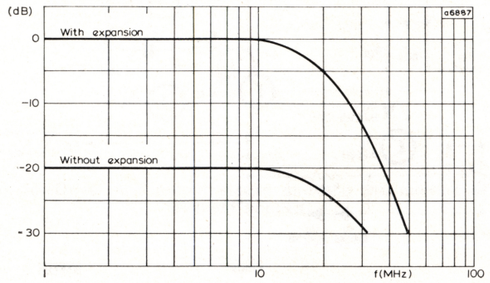


Fig. 16—Frequency response of the amplifier

COMPLETE CIRCUIT DIAGRAM

The complete circuit of the amplifier, incorporating all the features that have been discussed and indicating the supply voltage and interconnections of the respective stages, is given in Fig. 14. Variable resistor R_{26} has been provided for correct adjustment of the output stage.

PRACTICAL RESULTS

This section deals with the performance of the amplifier and the transistor operating conditions.

Input Conditions

The required sawtooth at the base of transistor TR_1 is shown in Fig. 15. The peak-to-peak voltage of 3·26V is applied across a resistance of 910Ω, giving a peak input current of 3·58mA.

The required peak voltage and current at the input of the driver stages are 1·25V at 6mA, corresponding to an input impedance of 210Ω.

Output Conditions

With a load capacitance of 11pF to earth on each side, a total output voltage swing of $2 \times 124 = 248$V is obtained, the rise time being 24ns. Measured with small input signals, the total rise time proved to be 20ns, with the x-expansion set to 10.

The frequency response of the amplifier is as shown in Fig. 16. Without expansion, the response is within 3dB from d.c. to 19MHz; with expansion the −3dB point is at 17MHz.

Fig. 17 shows the recorded trace for a sawtooth input giving a sweep rate of 0·5ns/mm.

Amplifier Fall Times

As previously stated, the short rise time of the amplifier is achieved at the cost of the fall time, which is less important. With x-expansion, a sweep rate of 0·5ns/mm requires an input signal lasting over 500ns, as can be seen from Fig. 18. As the input recovery time will be longer

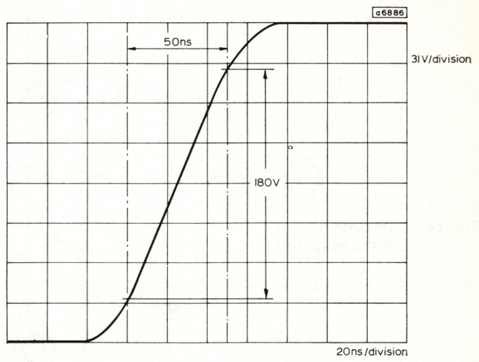


Fig. 17—The 1·8V/ns (0·5ns/mm) sweep as displayed on a sampling oscilloscope

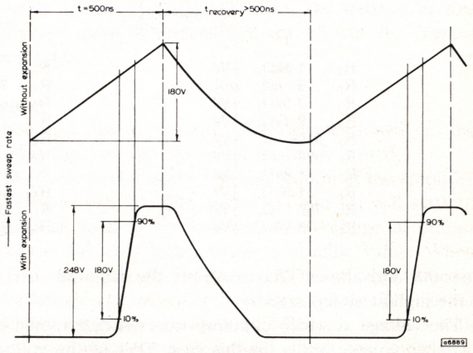


Fig. 18—Fastest normal sweep rates and corresponding recovery times

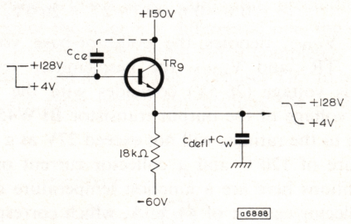


Fig. 19—Circuit elements which determine the fall time of TR_9

than 500ns, it is necessary only that the fall time of the amplifier be shorter than this. The total time depends almost exclusively on the separate fall times of the emitter follower TR_9 and of the inverting transistor TR_8 which form part of the output stage.

With a fast enough fall time at the input, the fall time of the emitter follower TR_9 is determined by the RC-time of its output; from the values indicated in Fig. 19, it can be calculated to be 184ns.

The transition frequency of transistor BFW45 being high enough, the fall time of the inverting transistor TR_8 is limited only by the RC-time of its output; with the component values indicated in the circuit of Fig. 20 it amounts to 84ns.

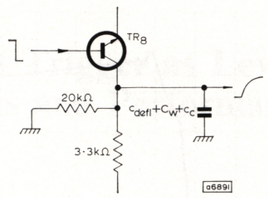


Fig. 20—Circuit elements which determine the fall time of TR_8

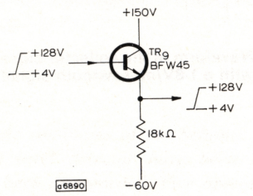


Fig. 21—Abstracted basic circuit of TR_9 for investigation of its output conditions

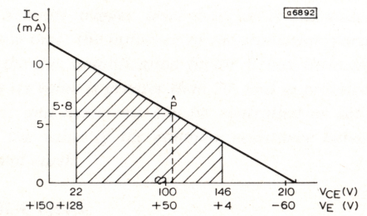


Fig. 22—Load line of transistor TR_9

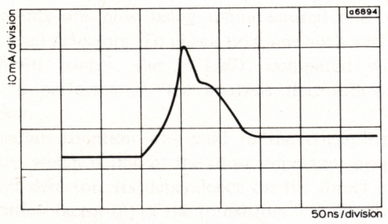


Fig. 23—Waveform of collector current of TR_9 with a sawtooth signal of 1·8V/ns

Transistor Operating Conditions

The BSX20 transistors (TR_1 to TR_6) are all operated well within their ratings and therefore present no problems. However, the operating conditions of the output transistors BFW45 (TR_7 to TR_9) must be carefully examined to make sure that they comply with the published ratings. The three transistors are operated under different conditions, and the dissipation of each is discussed separately.

Emitter Follower Output Transistor

The basic circuit is shown in Fig. 21 and the load line is given in Fig. 22. The voltage across the stage is 210V, and therefore the maximum current is 11·75mA. Bearing

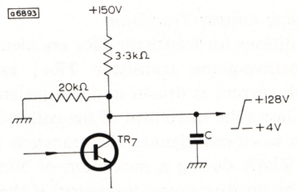


Fig. 24—Abstracted basic circuit of TR_7 (and TR_8) for investigation of the output conditions

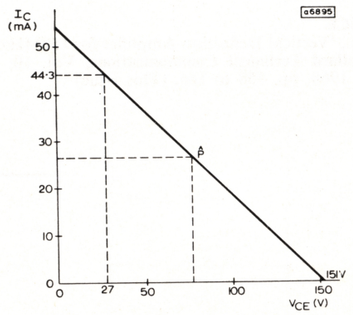


Fig. 25—Load line of transistor TR_7

in mind that, in the absence of an input signal, the shift control may be at any value between 22V and 146V, it will be seen that the conditions of maximum continuous dissipation may well occur: this dissipation is about 0·615W. At the fastest sweep rate the instantaneous dissipation is greater because of the additional load formed by the capacitances of the deflection electrodes, but the average dissipation is smaller.

The thermal resistance (junction to case) of the transistor is 20degC/W. Allowing for a heatsink with a thermal resistance to free air of 25degC/W, the junction temperature may reach 78°C at an ambient temperature of 50°C. This is well below the maximum permissible junction temperature of 200°C.

Fig. 23 shows the waveform of the collector current for the fastest sawtooth input signal. Under these conditions the peak current is 26mA; the maximum voltage is $150 - 4 = 146$V. These values, too, are within the published ratings.

Positive-going Output Transistor

The basic circuit of this transistor, which precedes the emitter follower, is shown in Fig. 24. The minimum collector-emitter voltage is 27V, and with a nominal output swing of 124V, the collector-emitter voltage reaches 151V. The maximum collector current is 44·3mA; the minimum current is negligibly small.

Fig. 25 shows the load line and the point of maximum dissipation P̂, amounting to almost 2W. As before, this dissipation may occur during the absence of an input signal. Assuming the same ambient temperature and heat sink as for the emitter follower discussed above, the maximum junction temperature may reach 140°C, which still is a safe value.

Negative-going Output Transistor

The conditions for transistor TR_8 are identical to those for the positive-going transistor TR_7, except that a greater peak current is drawn under transient conditions.

Fig. 26 shows the waveform of the collector current for a 0·5ns/mm sawtooth signal. The transient peak current may reach 90mA during a maximum of 50ns (as against 50mA for the positive-going transistor) if the input signal is a pulse instead of a sawtooth. This is within the ratings of the BFW45.

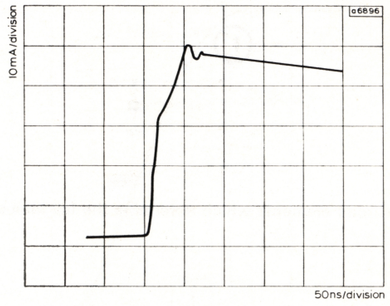


Fig. 26—Waveform of the collector current of TR_8 with a 1·8V/ns sawtooth signal

REFERENCE

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Schmitt Trigger as Level Detector : Analysis and Performance of FCL101

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The various static conditions of the Schmitt trigger circuit operating as a level detector have been analysed, and transients have been disregarded. Five operating states are identified and general equations derived which define the relationship between input voltage and current in each of them.

On this basis the performance of the integrated circuit FCL101 Schmitt trigger level detector is calculated. The results show that: the influence of the transistor parameters is small; the d.c. amplification factor β has little influence as long as its value is greater than 20, and in practice this is usually so; and hysteresis can be controlled or set by the choice of the value of the common resistance between the emitters and earth.

INTRODUCTION

Of the several types of regenerative amplitude comparator, the Schmitt trigger is perhaps the easiest to realise as an integrated circuit. Accordingly, integrated embodiments are now being manufactured and widely used as level detectors. To check how one such version of the Schmitt trigger, the FCL101, compared with its theoretical performance, the analysis that follows was undertaken.

Particular attention was paid to the triggering level hysteresis, which is one of the most important properties of a level detector. Its dependence on the direct current amplification factor (β) of the transistors was investigated, as was the effect of the common resistance between the emitters and earth. As the following analysis shows, the hysteresis is, in fact, not influenced to any great degree by variations in current amplification. The effect of the feedback resistance, on the contrary, is indeed large, but this is an advantage; it affords a convenient means of setting the hysteresis to the amount that may be required in practice.

GENERAL CIRCUIT

Consider first the Schmitt trigger circuit of Fig. 1, which is of sufficiently general form to cover most embodiments of this type of level detector. In practice E_1 and E_2 are usually equal, E_3 may be positive or negative with respect to earth, the resistance R_3 may be zero, or the collector of TR_2 may be shunted to earth by way of a load resistance. Since we are interested only in the static conditions of the circuit, we need not take into account the effect of a speed-up capacitor shunted across R_3. For purposes of analysis we shall focus our attention on the input characteristic; that is, on the behaviour of I_{B1}, the base current of TR_1, as a function of the input voltage V_A. As shown in Fig. 2, this characteristic has five clearly distinguishable regions, one of which is a region of negative resistance and accounts for the ability of the circuit to change rapidly from one stable state to another.

To begin with we shall assume that the circuit is so designed that when the input voltage V_A is zero, TR_2 is in saturation and TR_1 in cut-off. If the input voltage V_A

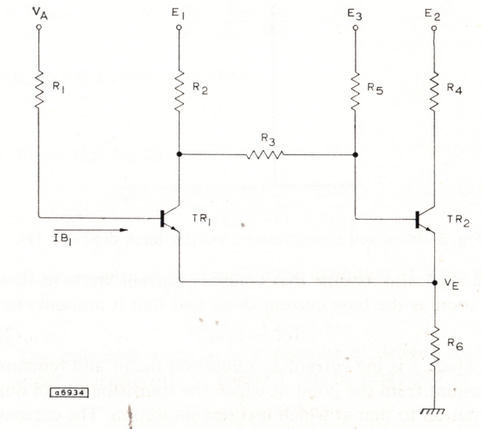

Fig. 1—General circuit of a Schmitt trigger

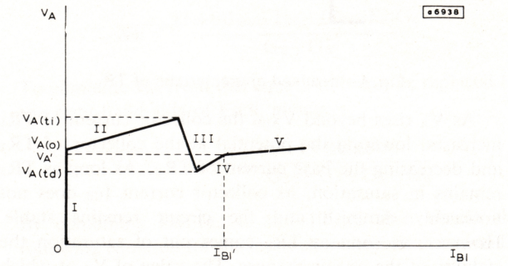

Fig. 2—Variation of base current I_{B1} with base voltage V_A of transistor TR_1 in the circuit of Fig. 1, illustrating the typical input characteristic of a Schmitt trigger

is increased (region I in Fig. 2), no current will flow until V_A equals the sum of the emitter-to-earth voltage V_E and the base-to-emitter voltage V_1 which is just sufficient to start base current flowing in TR_1. The point of transition from region I to region II is designated $V_{A(0)}$:

$$V_{A(0)} = V_E + V_1. \qquad \ldots(1)$$

For values of V_A higher than $V_{A(0)}$ TR_1 is conductive and behaves as a current generator (infinite internal impedance).

The diode formed by the emitter-base junction of TR_1 may be assumed to have an idealised characteristic as shown in Fig. 3, so its internal resistance can be disregarded.

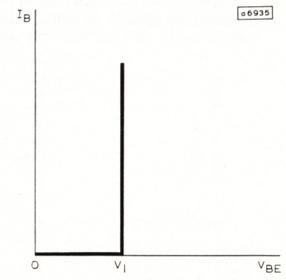

Fig. 3—Idealised characteristic emitter-base diode of TR_1

We shall also assume that collector current starts to flow as soon as the base current does, and that it amounts to:

$$I_{C1} = \beta I_{B1}, \qquad \ldots(2)$$

in which β is the current amplification factor and remains constant from the point at which the transistor comes out of cut-off to that at which it enters saturation. The current versus voltage characteristic for such an idealised transistor would be as shown in Fig. 4, in which E_s represents the saturation voltage, and the separations between the curves reflect equal increments of base current I_B.

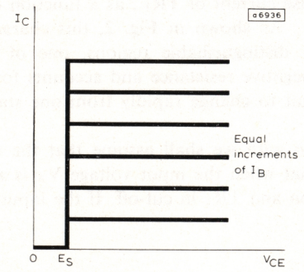

Fig. 4—Idealised characteristic of TR_1

As V_A rises beyond $V_{A(0)}$ the collector current of TR_1 increases, lowering the potential at the collector of TR_1 and decreasing the base current of TR_2. As long as TR_2 remains in saturation, its collector current I_{C2} does not noticeably diminish and the circuit remains stable. However, as soon as TR_2 comes out of saturation the stability of the circuit changes. The value of V_A at which this occurs, called the triggering level at increasing voltage, is designated $V_{A(ti)}$.

After the input voltage has reached the level $V_{A(ti)}$ both transistors behave as current generators (region III). As well as Eq.2 the following relationship applies:

$$I_{C2} = \beta I_{B2}, \qquad \ldots(3)$$

in which the current amplification factor β may be assumed to be identical to that of TR_1. (If both transistors are integrated on a single chip such an assumption is by no means unrealistic.)

In region III, where both transistors are actively conducting, the circuit becomes a two-stage amplifier with strong positive feedback so that the resistance between V_A and earth is negative. What this means is that, even if V_A decreases, the input current I_{B1} will continue to increase. The situation is an unstable one and persists only until transistor TR_2 enters cut-off ($I_{B2} = 0$). The value of V_A at which this occurs, called the triggering level at decreasing voltage, is designated $V_{A(td)}$. The voltage between the upper and lower broken lines is the triggering level hysteresis. Beyond $V_{A(td)}$ TR_2 remains in cut-off and TR_1 is actively conducting (region IV); the base current I_{B1} can be further increased only if V_A is increased.

If V_A is increased so far as to drive TR_1 into saturation the circuit enters a fifth region of operation which is the counterpart of region I; TR_1 is in saturation and TR_2 in cut-off.

Pertinent aspects of the five operating regions are summarised in Table 1.

In regions II, III, IV, and V the relationship between V_A and I_{B1} is expressed by the equation:

$$V_A = V_E + V_1 + I_{B1}R_1. \qquad \ldots(4)$$

In all regions the emitter voltage of both transistors with respect to earth is given by the equation:

$$V_E = (I_{B1} + I_{C1} + I_{B2} + I_{C2})R_6. \qquad \ldots(5)$$

If the circuit of Fig. 1 is redrawn in the simplified form of Fig. 5, Kirchhoff's laws can be applied to derive the following equation for I_{B2}:

$$I_{B2} = E_1G_{23} + E_3G_5 - (V_E + V_2)(G_{23} + G_5) - \\ - I_{C1}G_{23}/G_2 \qquad \ldots(6)$$

in which G_2, G_5, G_{23} etc. are substituted for $1/R_2$, $1/R_5$ and $1/(R_2+R_3)$ respectively, and V_2 represents the

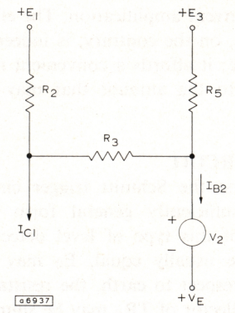

Fig. 5—Simplification of the circuit of Fig. 1

TABLE 1
Operating Regions of the Generalised Schmitt Trigger

Region	Condition	V_A	I_{B1}	I_{C1}	I_{B2}	I_{C2}
I	TR_1 cut off, TR_2 saturated	$\leqslant V_{A(0)}$	0	0	>0	$\frac{E_2-E_S-V_E}{R_4}$
II	TR_1 conducting, TR_2 saturated	$>V_{A(0)}$ $<V_{A(ti)}$	>0	βI_{B1}	>0	$\frac{E_2-E_S-V_E}{R_4}$
III	TR_1 and TR_2 both conducting, neither saturated	$<V_{A(ti)}$ $>V_{A(td)}$	>0	βI_{B1}	>0	βI_{B2}
IV	TR_1 conducting, TR_2 cut off	$>V_{A(td)}$	>0	βI_{B1}	0	0
V	TR_1 saturated, TR_2 cut off	$>V_{A(td)}$	>0	$\frac{E_1'-E_S-V_E}{R_2//(R_3+R_5)}$	0	0

The voltage E_1' amounts to $\{(R_3+R_5)E_1+R_2E_3\}/(R_2+R_3+R_5)$

base-to-emitter voltage of the conducting transistor TR_2 (just as V_1 represents that of TR_1, Fig. 3).

On the basis of these equations we can now derive expressions for the input characteristic, the relationship between I_{B1} and V_A, in each of the five regions.

DERIVATION OF THE INPUT CHARACTERISTIC

Essentially, the input characteristic is expressed by Eq.4; however, for our purposes, the quantity V_E in the right-hand side of that equation must be eliminated. Eq.5 tells us that V_E is a function of all the transistor currents flowing in the circuit. The next task, then, is to express I_{C1}, I_{B2} and I_{C2} as functions of I_{B1}. As can be seen from Table 1, I_{C1} presents no problem; moreover, by substituting in Eq.6, we can express I_{B2} in terms of I_{B1} and V_E. All that remains then is to solve for I_{C2}, and in regions III, IV, and V this is easily done. In regions I and II it is more difficult, because here V_E must be eliminated by combining Eq.5 with the relevant expressions from Table 1.

Proceeding on this basis we shall now develop the required expressions for the input characteristic in each of the five regions through which I_{B1} can move in response to changes in V_A.

Input Characteristic in Region I

From Table 1 we see that $I_{B1} = 0$ and $I_{C1} = 0$; the latter condition enables us to rewrite Eq.6 in the form:

$$I_{B2} = I_{B2(0)} = E_1G_{23} + E_3G_5 - \\ -(V_{E(0)} + V_2)(G_{23} + G_5), \qquad \ldots(6a)$$

in which, from Eq.5:

$$V_{E(0)} = (I_{B2(0)} + I_{C2(0)})/G_6, \qquad \ldots(5a)$$

the subscript 0 being used to designate values in region I. Again referring to Table 1 we find that in region I:

$$I_{C2(0)} = (E_2 - E_S - V_{E(0)})G_4,$$

in which substitution of the value of $V_{E(0)}$ expressed by Eq.5a, gives:

$$I_{C2(0)} = (E_2 - E_S - I_{B2(0)}/G_6)G_{46}. \qquad \ldots(7)$$

From Eqs.5a, 6a, and 7 it follows that:

$$V_{E(0)} = \frac{(E_2-E_S)G_4 + E_1G_{23} + E_3G_5 - V_2(G_{23}+G_5)}{G_{23}+G_4+G_5+G_6} \qquad \ldots(8)$$

which enables us to complete the definition of $V_{A(0)}$ given in Eq.1:

$$V_{A(0)} = V_{E(0)} + V_1. \qquad \ldots(1a)$$

The quiescent state is now completely defined and the input characteristic in region I can be expressed by:

$$0 \leqslant V_A \leqslant V_{A(0)} \qquad \ldots(9a)$$

$$I_{B1} = 0. \qquad \ldots(9b)$$

Input Characteristic in Region II

From *General Circuit* (page 175) we know that:

$$I_{C1} = \beta I_{B1}, \qquad \ldots(2)$$

and

$$V_E = (I_{B1} + I_{C1} + I_{B2} + I_{C2})/G_6. \qquad \ldots(5)$$

Moreover, Table 1 tells us that in region II:

$$I_{B1} > 0$$

and

$$I_{C2} = (E_2 - E_S - V_E)G_4.$$

Thus, by substitution of the foregoing equations for I_{C1} and I_{C2} in Eq.5, we can now write:

$$V_E = \frac{(1+\beta)I_{B1} + I_{B2} + (E_2 - E_S)G_4}{G_4 + G_6}.$$

To eliminate I_{B2} from this equation, it can be replaced by the right-hand side of Eq.6, giving:

$$V_E = V_{E(0)} + I_{B1}.\frac{1+\beta G_{23}/G_3}{G_{23}+G_4+G_5+G_6}. \qquad \ldots(10)$$

By combining Eqs.1a, 4, and 10 we then obtain the following equation for the input characteristic in region II:

$$V_A = V_{A(0)} + I_{B1}.\left(\frac{1}{G_1} + \frac{1+\beta G_{23}/G_3}{G_{23}+G_4+G_5+G_6}\right). \qquad \ldots(11)$$

Input Characteristic in Region III

From Eqs.6 and 6a it follows that:

$$I_{B2} = I_{B2(0)} - I_{C1}(G_{23}/G_2) + (V_{E(0)} - V_E)(G_{23}+G_5);$$

which, since $I_{C1} = \beta I_{B1}$, is equivalent to:

$$I_{B2} = I_{B2(0)} - \beta I_{B1}(G_{23}/G_2) + (V_{E(0)} - V_E)(G_{23}+G_5); \quad \ldots(6b)$$

moreover, since $I_{C2} = \beta I_{B2}$, Eq.5 can be rewritten:

$$V_E = (I_{B1}+I_{B2})(1+\beta)/G_6, \quad \ldots(5b)$$

in which I_{B2} can be replaced by the right-hand side of Eq.6b to give V_E in suitable form for use in Eq.4:

$$V_E = \frac{I_{B2(0)} + V_{E(0)}(G_{23}+G_5) + I_{B1}(1-\beta G_{23}/G_2)}{G_{23}+G_5+G_6/(1+\beta)}.$$

Whence, taking for $I_{B2(0)}$ the value given by Eq.6a we can find the form of Eq.4 that expresses the input characteristic in region III to be:

$$V_A = V_1 + \frac{E_1G_{23}+E_3G_5-V_2(G_{23}+G_5)}{G_{23}+G_5+G_6/(1+\beta)} + I_{B1}\left\{\frac{1}{G_1} + \frac{1-\beta G_{23}/G_2}{G_{23}+G_5+G_6/(1+\beta)}\right\} \quad \ldots(12)$$

on the basis of which we can now determine the triggering level at increasing voltage, $V_{A(ti)}$, and decreasing voltage, $V_{A(td)}$, and the difference between them, $\Delta V_{A(t)}$, the hysteresis.

Triggering Level at Increasing Voltage

The triggering level at increasing voltage is defined by the intersection of regions II and III; that is, by the common root of Eqs.11 and 12. To find this, we must first eliminate I_{B1} from both equations.

For the sake of brevity, we shall let:

$$G_{11} = \frac{G_{23}+G_4+G_5+G_6}{1+\beta G_{23}/G_3},$$

$$G_{111} = \frac{G_{23}+G_5+G_6/(1+\beta)}{1-\beta G_{23}/G_2},$$

and

$$V_{111} = \frac{E_1G_{23}+E_3G_5-V_2(G_{23}+G_5)}{G_{23}+G_5+G_6/(1+\beta)},$$

so that Eqs.11 and 12 can be rewritten in the form:

$$V_{A(11)} = V_{E(0)} + V_1 + I_{B1}(1/G_1 + 1/G_{11}), \quad \ldots(11a)$$

$$V_{A(111)} = V_1 + V_{111} + I_{B1}(1/G_1 + 1/G_{111}). \quad \ldots(12a)$$

Equating both functions, we find the value of I_{B1} at the point of intersection to be:

$$I_{B1(ti)} = (V_{E(0)} - V_{111})/(1/G_{111} - 1/G_{11}), \quad \ldots(13)$$

and the triggering level to be:

$$V_{A(ti)} = V_1 + \frac{V_{E(0)}(1/G_1+1/G_{111}) - V_{111}(1/G_1+1/G_{11})}{1/G_{111}-1/G_{11}}. \quad \ldots(14)$$

Triggering Level at Decreasing Voltage

The triggering level at decreasing voltage is reached when I_{B1} has increased to such an extent that $I_{B2} = 0$. Introducing this condition into Eq.6b enables us to find a direct relationship between V_E and I_{B1}. Since I_{B2} and I_{C2} are zero, Eq.5 gives us another useful relationship. From the two it is possible to solve for $V_{E(td)}$ and $I_{B1(td)}$, the emitter voltage and the base current of TR_1 at the decreasing voltage triggering level:

$$V_{E(td)} = \frac{E_1G_{23}+E_3G_5-V_2(G_{23}+G_5)}{\{\beta/(1+\beta)\}G_6G_{23}/G_2+G_{23}+G_5}, \quad \ldots(15)$$

and

$$I_{B1(td)} = V_{E(td)}G_6/(1+\beta). \quad \ldots(16)$$

By substituting these values in Eq.4, we obtain the following expression for the triggering level at decreasing voltage:

$$V_{A(td)} = V_1 + \{1+G_6/(1+\beta)G_1\}. \frac{E_1G_{23}+E_3G_5-V_2(G_{23}+G_5)}{\{\beta/(1+\beta)\}G_6G_{23}/G_2+G_{23}+G_5}, \quad \ldots(17)$$

or, in abbreviated form:

$$V_{A(td)} = V_1 + \{1+G_6/(1+\beta)G_1\}V_{E(td)}. \quad \ldots(17a)$$

Triggering Level Hysteresis

The hysteresis, $\Delta V_{A(t)}$, is the difference between the upper and lower triggering levels:

$$\Delta V_{A(t)} = V_{A(ti)} - V_{A(td)}. \quad \ldots(18)$$

Eqs.14 and 17 are so complex that using them to expand Eq.18 would lead us too far out of our way. In practical cases, the calculation must be carried out numerically (see *Input Characteristic of a Practical Circuit*, page 179).

Input Characteristic in Region IV

Since $I_{B2} = 0$ and $I_{C2} = 0$ (Table 1), Eq.5 can be simplified to:

$$V_E = (I_{B1}+I_{C1})R_6,$$

which, since $I_{C1} = \beta I_{B1}$, reduces to:

$$V_E = (1+\beta)I_{B1}/G_6. \quad \ldots(5c)$$

Substituted in Eq.4, this gives the input characteristic:

$$V_A = V_1 + I_{B1}\{1/G_1 + (1+\beta)/G_6\}. \quad \ldots(19)$$

Input Characteristic in Region V

As given in Table 1,

$$I_{C1} = \frac{(E_1' - E_S - V_E)(R_2+R_3+R_5)}{R_2(R_3+R_5)}$$

in which the voltage E_1' appearing in the numerator amounts to:

$$E_1' = \frac{(R_3+R_5)E_1 + R_2E_3}{R_2+R_3+R_5};$$

and, from Eq.5 since I_{B2} and I_{C2} are both zero, as before:

$$V_E = (I_{B1}+I_{C1})R_6.$$

By substitution, therefore, we can derive the expression:

$$V_E = \frac{E_1' - E_S}{1+G_6/G_2'} + I_{B1}/(G_6+G_2'), \quad \ldots(20)$$

in which $G_2' = G_2 + G_{35}$. Introducing the right-hand side of Eq.20 into Eq.4 then gives for the input characteristic:

$$V_A = V_1 + \frac{E_1' - E_S}{1+G_6/G_2'} + I_{B1}\left(\frac{1}{G_1} + \frac{1}{G_2'+G_6}\right). \quad \ldots(21)$$

The common root of Eqs.19 and 21 is the point of transition between the two regions. Letting V_A' and I_B' represent the values of V_A and I_B at this point, the simultaneous solution of the two equations gives:

$$I_{B1}' = \frac{E_1' - E_S}{\beta/G_2' + (1+\beta)/G_6}, \quad \ldots(22)$$

and

$$V_A' = V_1 + I_{B1}'\{1/G_1 + (1+\beta)/G_6\}. \quad \ldots(23)$$

INPUT CHARACTERISTIC OF A PRACTICAL CIRCUIT

Having derived the input characteristic in each of the five operating regions for a generalised case, we shall now apply the calculations to a practical Schmitt trigger. The circuit we shall consider is the monolithic integrated FCL101 with external resistors R_6 and R_7, as shown in Fig. 6. Table 2 summarises its typical operating characteristics as measured under the following conditions:

$E_1 = 6V$, $E_2 = 6V$, $E_3 = 0V$, $R_4 = 4{\cdot}7k\Omega$. The values of E_2 and R_4 are modified to 2·87V and 2·25kΩ by R_7 (4·3kΩ) which shunts the collector of TR_2 to earth.

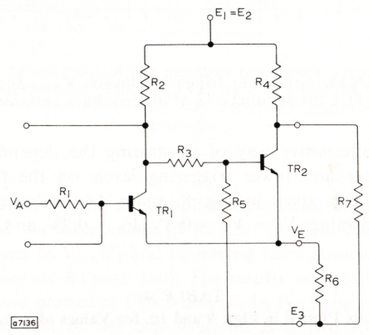

Fig. 6—FCL101 Schmitt trigger circuit

TABLE 2

Specified Performance of the FCL101 Schmitt Trigger at 25°C

R_6	10	50	100	200	Ω
$V_{A(ti)}$	0·85	0·95	1·10	1·30	V
$V_{A(td)}$	0·84	0·90	1·00	1·15	V
$\Delta V_{A(t)}$	10	50	100	150	mV

Data are tabulated for four different values of R_6: variations of this parameter, caused by changes in the value of R_6, strongly influence the upper and lower triggering levels, and the hysteresis.

Other resistance values in the circuit are: $R_1 = 1k\Omega$, $R_2 = 3{\cdot}3k\Omega$, $R_3 = 1k\Omega$, and $R_5 = 13k\Omega$.

The quantities V_1, V_2, E_S and β, which determine the behaviour of the transistors are not known. To begin with, therefore, we shall introduce only the known quantities into the previously derived expressions, leaving the unknown ones to be dealt with later.

The quantities that define the input characteristic are:

- $V_{A(0)}$, the input voltage at which TR_1 comes out of cut-off, Eqs.1a, 8;
- $V_{A(ti)}$, the triggering level at increasing voltage, Eq.14;
- $I_{B1(ti)}$, the base current of TR_1 at $V_{A(ti)}$, Eq.13;
- $V_{A(td)}$, the triggering level at decreasing voltage, Eq.17;
- $I_{B1(td)}$, the base current of TR_1 at $V_{A(td)}$, Eq.16;
- V_A', the input voltage at which TR_1 enters saturation, Eq.23;
- I_{B1}', the base current of TR_1 at V_A', Eq.22.

These are sufficient to determine both the upper and lower limits of regions, I, II, III and IV, but only the lower limit (V_A', I_{B1}') of region V. However the slope of the line in region V is implicit in Eq.21, so its position can be established easily by substituting $I_{B1} = 0$ in that expression.

By introducing the appropriate numerical values into the expressions that define them, the following constants can now be evaluated:

$E_1' = 4{\cdot}86V$
$R_2' = 2{\cdot}67k\Omega$
$G_{11} = (0{\cdot}755+G_6)/(1+0{\cdot}2325\beta)$mmho
$G_{111} = \{0{\cdot}3095+G_6/(1+\beta)\}/(1-0{\cdot}7675\beta)$mmho
$V_{111} = (1{\cdot}39-0{\cdot}3095V_2)/\{0{\cdot}3095+G_6/(1+\beta)\}V.$

With the aid of these and the other numerical values given we can now find, from Eq.8:

$$V_{E(0)} = (2{\cdot}65-0{\cdot}446E_S-0{\cdot}3095V_2)/(0{\cdot}755+G_6),$$

from Eq.1a:

$$V_{A(0)} = V_1 + V_{E(0)},$$

from Eq.14:

$$V_{A(ti)} = V_1 + \frac{V_{E(0)}(1+1/G_{111}) - V_{111}(1+1/G_{11})}{1/G_{111}-1/G_{11}},$$

from Eq.17:

$$V_{A(td)} = V_1 + \left(1+\frac{G_6}{1+\beta}\right).\frac{1{\cdot}39-0{\cdot}3095V_2}{\beta/(1+\beta)0{\cdot}7675G_6+0{\cdot}3095},$$

from Eq.22:

$$I_{B1}' = \frac{4{\cdot}86-E_S}{(1+\beta)(2{\cdot}67+1/G_6)-2{\cdot}67},$$

and from Eq.23:

$$V_A' = V_1 + I_{B1}'\{1+(1+\beta)/G_6\},$$

in all of which voltages are expressed in V, conductances in mmho, and currents in mA.

These expressions make certain dependences of the input characteristic apparent.

Dependence on V_1

All the expressions for characteristic voltages contain a term V_1, the influence of which is to shift the input characteristic vertically. However, in the equation for hysteresis, $\Delta V_{A(t)} = V_{A(ti)} - V_{A(td)}$, the term V_1 vanishes, so regardless of any shift in the characteristic due to variation of V_1 the hysteresis is unaffected. In practice, the variation of V_1 may amount to a few tenths of a volt.

Dependence on V_2

The influence of V_2 is largest on V_{111} and $V_{A(td)}$, in the equations for which it appears in the numerator. Like V_1, V_2 may also vary by a few tenths of a volt, but its influence is negligible. Even if it varies by as much as half a volt, the resulting variation of V_{111} and $V_{A(td)}$ amounts only to about 1 per cent.

Dependence on E_S

The saturation voltage E_S, which may also vary by a few tenths of a volt, appears only in the equation for $V_{E(0)}$ and its influence is small. Even if E_S varies by as much as half a volt, the value of $V_{E(0)}$ is not altered by more than 1 per cent.

Dependence on R_6

From the fact that the term G_6 appears in several of the

equations, it is reasonable to expect that changing the value of R_6 from 200Ω to 10Ω would significantly affect the input characteristic. To find out how great the effect is, the simplest course is to substitute appropriate numerical values for the quantities V_1, V_2, E_S and β, and to work out the results. Realistic numerical values are:

$$V_1 = V_2 = 0{\cdot}8V \qquad E_S = 0{\cdot}2V \qquad \beta = 50$$

With these as a basis, the values in Table 3 have been calculated; for the sake of comparison, the published values of $\Delta V_{A(t)}$ are also tabulated alongside the calculated ones.

TABLE 3

Calculated Values Compared with Published Values for $\Delta V_{A(t)}$

R_6	200	100	50	10	Ω
R_{11}	2200	1170	560	125	Ω
R_{111}	−91·5	−73·8	−53·1	−16·4	kΩ
V_{111}	2·80	2·26	1·63	0·50	V
$V_{E(0)}$	417	223	116	23	mV
$V_{A(ti)}$	1·299	1·083	0·960	0·856	V
$I_{B1(ti)}$	25·5	27·2	28·2	29·0	μA
$V_{A(td)}$	1·109	0·974	0·902	0·845	V
$I_{B1(td)}$	27·5	28·6	29·2	29·7	μA
$\Delta V_{A(t)}$ calc.	190	109	58	11	mV
$\Delta V_{A(t)}$ publ.	150	100	50	10	mV

Input characteristics reflecting these values are indicated in Fig. 7; the whole characteristic is drawn only for $R_6 = 200\Omega$, with an assumed β of 50. Region III is also drawn for all the tabulated values of R_6 to show its effect on the hysteresis. The circuit ceases to operate as a Schmitt trigger as soon as the negative resistance in region III disappears, which, according to Eq.12a, is the case when $1/G_1+1/G_{111} = 0$. From the equation in which G_{111} is defined (page 179), it follows that if $\beta = 50$ the value of R_6 at which this occurs is about half an ohm, and if $\beta = 20$ it is about two thirds of an ohm.

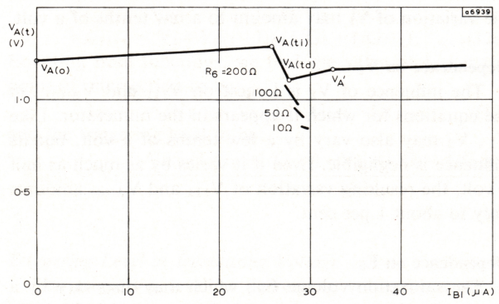

Fig. 7—Input characteristic of the FCL101

On the other hand, if $R_6 = 10\Omega$, the negative resistance would vanish only if the value of β were to be as low as 10; and for $R_6 = 200\Omega$, β must be no more than about 3 for the negative resistance to vanish. From these figures we can draw the conclusion that, in respect of ensuring its operation as a level detector, the FCL101 has been generously designed.

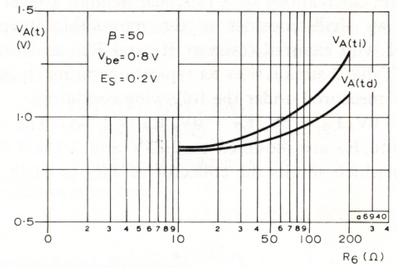

Fig. 8—Upper and lower triggering levels, $V_{A(ti)}$ and $V_{A(td)}$, of the FCL101 as functions of the feedback resistance R_6

An alternative way of illustrating the dependence of the upper and lower triggering levels on the feedback resistance is given in Fig. 8, again on the basis of the assumed values $V_1 = V_2 = 0{\cdot}8V$, $E_S = 0{\cdot}2V$, and $\beta = 50$.

TABLE 4

Results Plotted in Figs. 9 and 10, for Values of β and R_6

R_6 (Ω)	β	$V_{A(ti)}$ (V)	$I_{B1(ti)}$ (μA)	$V_{A(td)}$ (V)	$I_{B1(td)}$ (μA)	$\Delta V_{A(t)}$ (mV) calc.	publ.
200	∞	1·269	0	1·076	0	193	150
	100	1·284	12·8	1·092	13·7	192	
	70	1·290	18·3	1·098	19·6	192	
	50	1·299	25·5	1·109	27·5	190	
	40	1·305	31·5	1·116	34·4	189	
	30	1·316	41·6	1·130	45·8	186	
	20	1·339	61·0	1·158	68·8	181	
	10	1·400	115	1·236	136	164	
100	∞	1·053	0	0·943	0	110	100
	100	1·068	13·7	0·959	14·2	109	
	70	1·074	19·4	0·965	20·4	109	
	50	1·083	27·2	0·974	28·6	109	
	40	1·090	33·7	0·982	36·0	108	
	30	1·101	45·0	0·994	47·4	107	
	20	1·123	65·0	1·022	71·4	101	
	10	1·185	124	1·100	143	85	
50	∞	0·932	0	0·873	0	59	50
	100	0·947	14·2	0·888	14·6	59	
	70	0·953	20·2	0·894	20·8	59	
	50	0·960	28·2	0·902	29·2	58	
	40	0·968	35·0	0·911	36·4	57	
	30	0·980	46·0	0·924	48·6	56	
	20	1·002	68·0	0·951	74·0	51	
	10	1·065	128	1·025	145	40	

Dependence on Current Amplification Factor

With numerical values substituted in the equations for $I_{B1(ti)}$, $V_{A(ti)}$, $I_{B1(td)}$, and $V_{A(td)}$ (Eqs.13, 14, 16 and 17), the dependence of the negative resistance part of the input

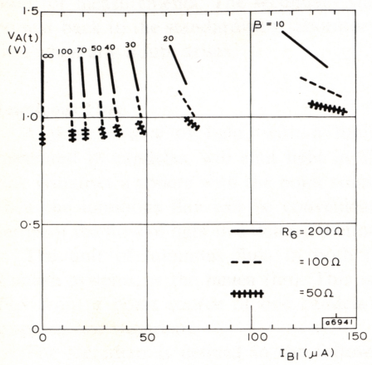

Fig. 9—Displacement of the negative resistance parts of the input characteristic of the FCL101 as a function of the d.c. amplification factor β, with the feedback resistance as parameter

characteristic on the d.c. amplification factor β has been calculated for three values of R_6: 50, 100 and 200Ω (the same values of V_1, V_2 and E_S having been assumed as in *Dependence on R_6* page 180). The results are tabulated in Table 4 and plotted in Figs.9 and 10. In Fig.9 the negative resistance part of the characteristic is drawn for eight values of β, from 10 to ∞, at each of the three values of R_6; in Fig.10 the hysteresis is plotted as a function of β with R_6 as parameter. From the two graphs it is clear that as long as the d.c. amplification factor is greater than 20 (which will nearly always be the case in practice), it has little influence on the triggering level or hysteresis of the FCL101 level detector.

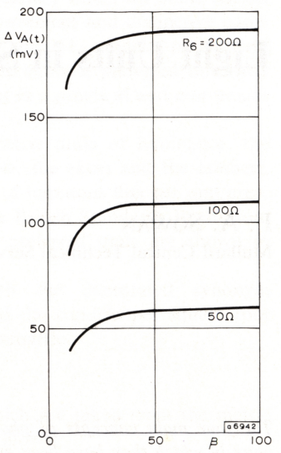

Fig. 10—Triggering level hysteresis of the FCL101 calculated as a function of the d.c. amplification factor β, with the feedback resistance as parameter

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Light Units in SI

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The four main concepts of photometry are discussed, the units in which they have been evaluated are examined, and the exclusive use of the four photometric units of the Système International d'Unités (SI) is recommended. Conversion tables from other systems to SI are given.

INTRODUCTION

The present strong drive toward metrication, and in particular toward the use of SI units (Système International d'Unités), brings few problems to the electronics engineer working on purely electrical or electronic projects; but as electronics penetrates other engineering or technological fields, certain non-electrical units have to be used. In television engineering, in oscilloscopy, and in a growing number of other fields, it is necessary to use the photometric units derived from the basic SI unit the candela.

PHOTOMETRIC UNITS

One often finds some confusion about photometric units. Many engineers are familiar with a small number of units (some of them, perhaps, obsolete), but are uncertain about the rest. Discussions, therefore, tend to be at cross-purposes and to be complicated by attempts at conversion; and articles or data sheets are readily understood by only a proportion of their readers or users.

This state of affairs is not surprising, since the basic concepts of photometry have confusingly similar names; and a great number of units have been devised from time to time—some metric and some English—with inconvenient and unmemorable conversion factors which are often ruthlessly rounded off to 'about 10'.

There are so many units, and such a variety of usage, often extending to the employment of units taken haphazardly from metric and English systems, that any attempt to sort out the confusion must take the form of specific recommendations. This article will therefore discuss the preferred SI units for the main photometric quantities, and then provide conversion tables covering all the units that are likely to be still in use.

The four photometric units in SI are the candela (a basic unit of the system, along with the metre, kilogramme, second, ampere, and degree Kelvin), the lumen, the lux, and the candela per square metre (at one time conveniently known as the nit). These four units relate to the four quantities that have to be defined and evaluated in photometry, namely:

Luminous intensity: the 'candle power' of a light source (which is assumed to be a point source, although, of course, this is not realisable in practice).

Luminous flux: the flow of light from the source, related to the solid angle over which measurement is made.

Illumination: the luminous flux falling on a surface, expressed as luminous flux per unit area.

Luminance: the luminous intensity of an illuminated surface, usually expressed as luminous intensity per unit area.

Luminous Intensity

The popular expression 'candle power', which refers to the idea of brightness (a deprecated term if it is not more closely defined), is now supplanted by the term 'luminous intensity'.

There is no confusion of units here. On 1 January 1948, a multiplicity of 'candles' and lamps (English, German, Pentane, Methven, Carcel, Vernon-Harcourt, International, and Hefner-Alteneck, to say nothing of the Bougie Decimale), were superseded by the 'new candle' or **candela** (cd), which has won international recognition.

The candela is evaluated in terms of the luminous intensity of a black body at the temperature of solidification of platinum. A full definition is given by Kaye and Laby (13th edition, page 10), and the practical setting-up and observation of this primary standard is fully discussed in J. W. T. Walsh's *Photometry* and in *Photometric Standards and the Unit of Light* by J. S. Preston.

A number of national laboratories have evaluated the candela in this way, and they have set up secondary standards in the form of tungsten lamps, of special design, calibrated against the primary standard. There are slight experimental discrepancies between the standard candelas maintained in various countries, but these are too small to affect practical photometry.

The only real difficulty about the candela is that lamps blacken with use, and their filaments undergo changes which alter the light output. It is therefore essential to reserve one or two 'secondary standard' lamps strictly for the purpose of calibrating the 'working standards' that are

used for measurements. The secondary standards should be sent back to the standardising laboratory for recalibration when any doubt arises.

Luminous Flux

A point source of light, with a luminous intensity measured in candelas, will emit light in all directions. If one visualises a sphere with the point source at its centre, then the luminous flux can be conveniently specified in terms of the flow of light in a defined section of the sphere.

The unit of luminous flux, in both the metric and English systems, is the **lumen** (lm). This is the luminous flux from a point source of one candela within a solid angle of one steradian.

The steradian is defined in the following manner. If the radius of a sphere is r, and an area equal to r^2 is marked on the surface of the sphere, then the solid angle subtended by this area is one steradian. It is clear that the definition is independent of the actual magnitude of r. The radius may be a foot or a metre; the solid angle remains the same. It is also seen that the complete sphere comprises 4π steradians—that is, 12·57. Thus the total luminous flux from a point source of one candela is 12·57 lumens.

Illumination

When the luminous flux falls on the inner surface of the sphere, the surface is illuminated. Illumination is defined in terms of luminous flux and the area of the surface. Much photometry, of course, is concerned with luminous flux falling on flat surfaces. The error entailed in ignoring the difference between a flat surface and a spherical surface can often be ignored; but if the angle which the surface subtends is large, then the necessary correction factor should be used. Tables are available in H. A. E. Keitz's *Light Calculations and Measurements*. The error is 0·4% when the half-apex angle of the cone of light is 4°, and 2·3% when it is 10°.

The metric unit of illumination is the **lux** (lx), which is the illumination produced by one lumen falling on an area of one square metre. It follows that an illumination of 1 lux is produced on an area of 1 square metre at a distance of 1 metre from a point source of 1 candela.

An alternative (but not preferred) metric unit is the phot, which is one lumen per square centimetre. One phot is equivalent to 10 000 lux. It will be noticed that, as the area is smaller, the illumination produced by one lumen is greater.

Illumination can, of course, be defined in terms of any unit of area. Thus the English unit is the foot-candle or lumen per square foot, which is approximately equal to 10 lux. There are also the sea-mile candle and the nox.

Luminance

A surface, which is either illuminated or self-luminous, will appear to an observer to be more or less bright. Brightness, however, is a subjective concept, and the term luminance is used for the definable quantity.

Luminance is expressed in terms of luminous intensity ('candle power') per unit area. The metric unit is the candela per square metre (cd/m²) which for some reason has been deprived of its convenient and distinctive name the *nit*. Occasionally the stilb (1 candela per square centimetre) is used. The stilb is not a preferred unit (it is deprecated in BS233), but it is a practical and convenient unit for some purposes.

There are two other metric units of luminance, the apostilb (with a submultiple, the skot) and the lambert, which are defined in terms of luminous flux per unit area. They are deprecated by the British Standards Institution. Their relationships to the preferred units are shown in the table.

The foot-lambert (with the deprecated synonym equivalent foot-candle) and the candela per square foot are the English units of luminance.

METRIC UNITS (SI)

The preferred units, which are taken from the metric system, are, therefore, as follows:

	Unit	*Abbreviation*
Luminous intensity	candela	cd
Luminous flux	lumen	lm
Illumination	lux (1m/m²)	lx
Luminance	cd/m²	—

Illumination and luminance are evaluated in units that contain an areal dimension which may, of course, be defined in metric or English units. It is here, therefore, that units have proliferated, and that differing and even mixed usages have come into being. To help toward the reduction of practice to the single, preferred, metric system, conversion tables are given for the non-preferred or deprecated units of illumination and luminance that are still in common use. The preferred units are the lux and the cd/m² (nit).

THE BACKGROUND OF PHOTOMETRY

Photometry is a sufficiently, but not wholly, exact science. Its units are necessarily expressed in terms of light—that is, the part of the electromagnetic spectrum which excites the sensation of vision. The spectral response of the eye is not equal throughout this narrow frequency band, so that photometry has not so far been directly based on absolute units of energy. Further, the spectral response curve of any particular eye differs from that of other eyes (left eyes may markedly differ from right eyes) and is not even constant with time or with different levels of luminous flux. Finally, the eye is subject to fatigue, afterimages, and the effect of glare; and it is relatively slow to adapt to changed illumination.

The dependence of photometry on the characteristics of the eye is summed up on page 82 of Walsh's *Photometry*: 'It is more than likely that in many of the branches of practical photometry there are unrecognised sources of uncertainty which may, later on, be traced to some at present unsuspected phenomenon of vision'.

In present-day photometry the tendency is to use an artificial eye consisting of a suitable photo-electric device combined with filters that produce a spectral response curve which approximates to that of the internationally agreed 'standard observer'. The National Physical Laboratory is, however, investigating the possibility of placing

the unit of light on a radiometric basis. An account of this work is given by J. S. Preston.

It should be noted that the measurement of infra-red or ultra-violet radiation is *not* part of photometry in the strict sense, and that such measurements are made in terms of ordinary physical units.

SUMMARY

No attempt has been made in this article to give either a rigorous or a complete account of photometric principles. It is, indeed, probably impossible to write a short and simple guide to photometry. The knowledgeable reader will, therefore, be able to point out many inadequacies and silences. These are deliberate.

Our object has been to disentangle the confusion that tends to surround the main photometric units, and to recommend the use of a coherent system. Readers who wish to go further will find the bibliography useful.

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ILLUMINATION

		lux	phot	foot-candle
1 lux (1m/m²)	=	1	10^{-4}	$9{\cdot}29\times10^{-2}$
1 phot (1m/cm²)	=	10^{4}	1	929
1 foot-candle (1m/ft²)	=	10·76	$10{\cdot}76\times10^{-4}$	1

LUMINANCE

		cd/m² (nit)	stilb	cd/ft²	apostilb	lambert	foot-lambert
1 cd/m² (nit)	=	1	10^{-4}	$9{\cdot}29\times10^{-2}$	π	$\pi\times10^{-4}$	0·292
1 stilb (cd/cm²)	=	10^{4}	1	929	$\pi\times10^{-4}$	π	2920
1 cd/ft²	=	10·76	$1{\cdot}076\times10^{-3}$	1	33·8	$3{\cdot}38\times10^{-3}$	π
1 apostilb (1m/m²)	=	$1/\pi$	$1/(\pi\times10^{-4})$	$2{\cdot}96\times10^{-2}$	1	10^{-4}	$9{\cdot}29\times10^{-2}$
1 lambert (1m/cm²)	=	$1/(\pi\times10^{-4})$	$1/\pi$	296	10^{4}	1	929
1 foot-lambert or 'equivalent foot-candle' (1m/ft²)	=	3·43	$3{\cdot}43\times10^{-4}$	$1/\pi$	10·76	$1{\cdot}076\times10^{-3}$	1